# Application Note

## Interface Solutions for Lumineq TFEL Displays


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## A. TFEL INTERFACE OVERVIEW

The majority of Lumineq TFEL display products use an interface consisting of the following digital inputs:

- VS, to indicate the start of a frame of data
- HS, to indicate the start of a row of data
- VCLK, to clock in the pixel data
- VID, the pixel data

The "VID" can be a single input, two inputs, four inputs, or eight inputs depending on the display model and, in some cases, the mode setting of the display. Thus the data for either one, two, four, or eight pixels is clocked in on every active clock edge.

Most common is the 4 bit interface, where there are 4 bits of parallel data per clock. This 4 bit interface was first used, and continues to be used, in the monochrome LCD industry, though the LCD terminology is typically different (e.g., FRM = VS, LP or LOAD = HS, CP = VCLK).

The 1 and 2 bit interfaces are similar to the 4 bit interface but with slight timing differences and with fewer bits of pixel data clocked in per clock.

The 8 bit interface is based on a dual panel scheme popularized in the early days of large passive LCDs, where data for four pixels in the upper half of the displayed are clocked in simultaneously with data for four pixels from the bottom half of the display.

All models except the EL320.240 FA3 are monochrome. For the multicolor FA3, 4 bits per pixel are required to define the pixel color.

The EL240.128.45 has a built-in RAiO RA8835A video controller IC. The interface of the RAiO RA8835A is designed to connect to an 8 bit microprocessor bus which is used to pass data and commands to the display.

## B. SUMMARY OF TFEL INTERFACES BY DISPLAY FAMILY

The table below summarizes the TFEL interface type for each TFEL product family. Refer to the appropriate Operation Manual for details on each product's interface timing and requirements.

| Display Family | 1 bit | 2 bit | 4 bit | 4 bit color | 8 bit dual | Other/Notes |
|---|---|---|---|---|---|---|
| EL160.80.50 | | | X | | | |
| EL160.120.39 | | | X | | | |
| EL240.128.45 | | | | | | Microprocessor interface |
| EL320.240.36 | | | X | | | |
| EL320.240.36 HB | | | X | | | |
| EL320.240 FA3 (Multicolor) | | | | X | | Accepts CMOS AMLCD VGA or QVGA timing |
| EL320.256 F Series | X | X | | | | |
| EL480.240 PR | | | X | | | |
| EL512.256 H Series | X | X | | | | |
| EL640.200 SK | | | X | | X | |
| EL640.400 C Series | X | X | | | | Also accepts CMOS VGA "feature connector" timing |
| EL640.480 AF | | | | | X | |
| EL640.480 AG | | | | | X | |
| EL640.480 AM | | | | | X | |

## C. INTERFACE SOLUTION CATEGORIES

There are several ways to generate the required interface signals:

- Embed a video controller IC in your custom board and use your microprocessor or PC bus to communicate with the video controller IC
- Select a microprocessor that contains an integrated flat panel controller
- Use a video board that can drive TFEL displays
- Select a Single Board Computer that has the required flat panel video outputs
- Use a video converter board (e.g., an LVDS to TFEL converter board if LVDS video is already available)

## D. SUMMARY OF INTERFACE SOLUTIONS

Below is a summary of interface solutions available for TFEL displays.

Most of the solutions for 4 bit interfaces would work for 1 or 2 bit interfaces by ignoring unused bits if care was taken during software development to insert null data into the unused bit locations.

The following list is not exhaustive and other solutions exist. Also note that most of these solutions have not been verified by Beneq Products Oy.

## 1. Embedded Controller ICs

Epson S1D13705 (supports 1, 2, 4, and 8 bit interface products and FA3)

The S1D13705 is a controller IC that can display text and graphics. The IC interfaces to a microprocessor or PC I/O via a standard 8 bit Intel 8080 or Motorola 6800 bus. The IC can display layered text and graphics, scroll the display in any direction and partition the display into multiple screens. It also stores text, character codes and bit-mapped graphics data in external frame buffer memory.
http://www.epson.jp/device/semicon_e/product/lcd_controllers/index.htm

Epson S1D13700 (supports 4 bit interface products and FA3)

The S1D13706 is a controller IC that can display text and graphics on both monochrome and color displays. The IC interfaces to a microprocessor or PC I/O via a standard 8 bit Intel 8080 or Motorola 6800 bus.
http://www.epson.jp/device/semicon_e/product/lcd_controllers/index.htm

RAiO RA8835 (supports 4 bit interface products)

Designed as a drop-in replacement for the now obsolete Epson S1D13305 and similar to the S1D13700 and S1D13705, the RA8835 is a controller IC that can display text and graphics and interfaces to a microprocessor via a standard 8 bit bus. (See the note at the end of this paper for a discussion of a RA8835 discrepancy.)
http://www.raio.com.tw/E%20version/e_product.8835.htm

Other potential suppliers

Amulet Technologies
http://www.amulettechnologies.com/

## 2. Embedded Microprocessors with on-board Controller

Potential suppliers

Freescale
http://www.freescale.com/

Prosoft Ltd.
http://www.prosoft.ru/

## 3. Video Boards

Potential suppliers

Advanced Digital Logic
http://www.adl-usa.com/

Reach Technology
http://www.reachtech.com/

Digital View
http://www.digitalview.com/

Prosoft Ltd.
http://www.prosoft.ru/

## 4. SBCs and PC/104 Solutions

Potential suppliers

Advantech
http://www.advantech.com/products/

F&S Electronic
http://www.fs-net.de/cms/index.php

Eurotech
http://www.applieddata.net/

Prosoft Ltd.
http://www.prosoft.ru/

## 5. Miscellaneous Solutions

LVDS to TFEL interface (supports 4 and 8 bit interface products)

Lumineq has an LVDS to TFEL interface card which supports Lumineq 4 bit and 8 bit TFEL displays. The interface card converts 4 channel LVDS video data into the data format required by Lumineq TFEL displays.
http://lumineq.com/sites/default/files/product/fields/field_product_data_sheet/tfel_lvds_adapter.pdf

Lumineq TFEL Development Kit

Consists of a display controller board, display cable and Development Kit CD-ROM. Can be used in demo mode to display bmp files when connected to a PC's parallel port, or can be used in engineering mode with the engineer's microprocessor or I/O card communicating with the on-board Epson S1D13700 controller. Kits are available for the following TFEL display families: EL160.80.50, EL160.120.39, EL320.240.36, EL320.240.36 HB, EL640.200 SK.
http://lumineq.com/sites/default/files/product/fields/field_product_data_sheet/microp_bus_dev_kit_0.pdf

ASIC solution

Some Lumineq customers have developed embedded proprietary ASICs to drive their TFEL display. This solution is engineering intensive and requires relatively high volumes in order to justify the cost of the ASIC design.

## E. INTERFACE CONSIDERATIONS

The brightness of a TFEL display is directly proportional to the frame rate at which the panel is driven. In most TFEL products (those without a frame buffer) the panel frame rate is the same as the VS frequency. Thus for maximum brightness, the implementer must take care to select a solution that can provide a VS frequency near the specified maximum frame rate. See the TFEL product's manual for maximum frame rate.

Some displays have frame buffers that allow high panel frame rates—and thus high brightness—regardless of the input VS frequency. The following models have frame buffers (thus for these models the brightness is not related to VS frequency): EL320.240.36 HB, EL320.240 FA3, EL640.200 SK (4 bit mode only) and EL240.128.45.

A potential side effect with frame buffers occurs when the incoming pixel data has been frame dithered or spatially dithered in order to provide gray scale functionality. (Some video controllers can generate limited gray scale on monochrome displays by either moving a pixel around periodically [spatial dithering] or by turning the pixel on only during a portion of the active frames [frame dithering.]) The asynchronous relationship between the frame buffer and the gray scale dithering scheme can cause objectionable visual artifacts such as flicker.

Note that gray scales generated by frame dithering can cause visual artifacts even on displays that do not contain frame buffers. Typically the user can generate two or three levels of gray scale via frame dithering without significant visual artifacts, depending on the frame rate. With higher display frame rates, the visual artifacts are less severe. Also, avoiding large blocks of gray scale areas will make the visual artifacts more tolerable.

## F. NOTE on RAiO RA8835

Though designed as a drop-in replacement for the now obsolete Epson S1D13305, the RA8835 exhibits a timing anomaly: the first 3 clock widths on the XSCL (VCLK) are shorter than the rest: e.g., only 100ns long before changing to 200ns-300ns (see Figure 1 below). This created a timing issue on a test display such that the first few sets of data were not displayed. Slower Vclk rates or different register parameters may be required to allow the RA8835 to be used without side effects.

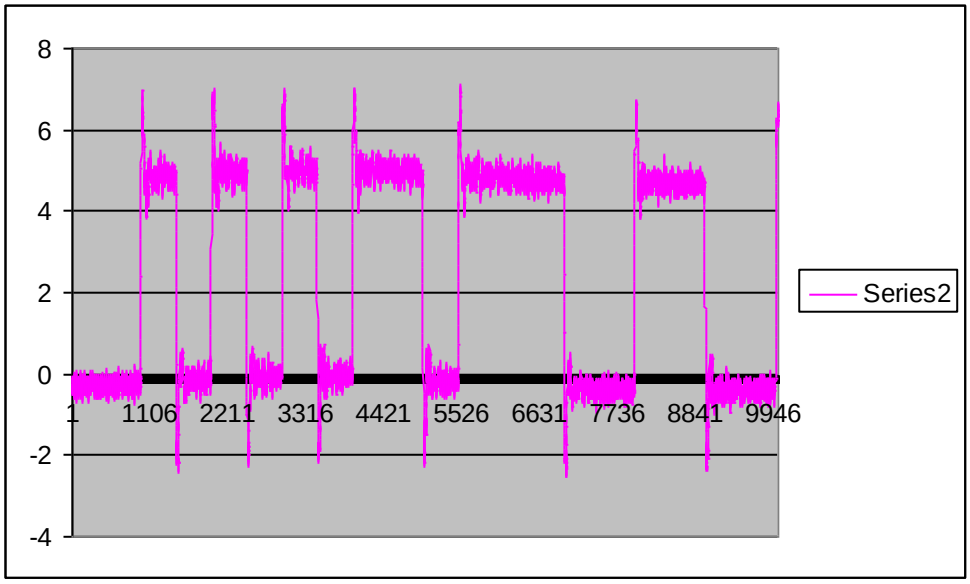


**Figure 1. RA8835 Start of VCLK**

If improving the timing is not effective it is also possible to fill the first 3 sets of data with null data and increase the horizontal pixel count by 12.