# EL640.400-CB1/CB3 and -CD4
## Operation Manual

## Table of contents:

# 1 Product profile

The EL640.400-CB1/3 and -CD4 displays are VGA compatible high-resolution Thin Film Electroluminescent (TFEL) flat panel displays. They feature an integrated DC/DC converter, and their compact dimensions save space that allows addition of features or reduction in overall size. The three displays are mechanically identical.

The displays are timing-compatible with EL640.400-C3/CD3 displays and signal compatible with VGA Feature Connector supporting the 350 and 400 line VGA modes. They may be driven at frame rates up to 72 Hz.

The displays require +5 $V_{DC}$ and +12 or +24 $V_{DC}$ power input and four basic input signals to operate:

1. Video Data or pixel information
2. Video Clock, pixel clock, or dot clock
3. Horizontal Sync or Blanking
4. Vertical Sync

# 2 EL technology

Lumineq® TFEL displays consist of an electroluminescent glass panel and a mounted circuit board with control electronics.
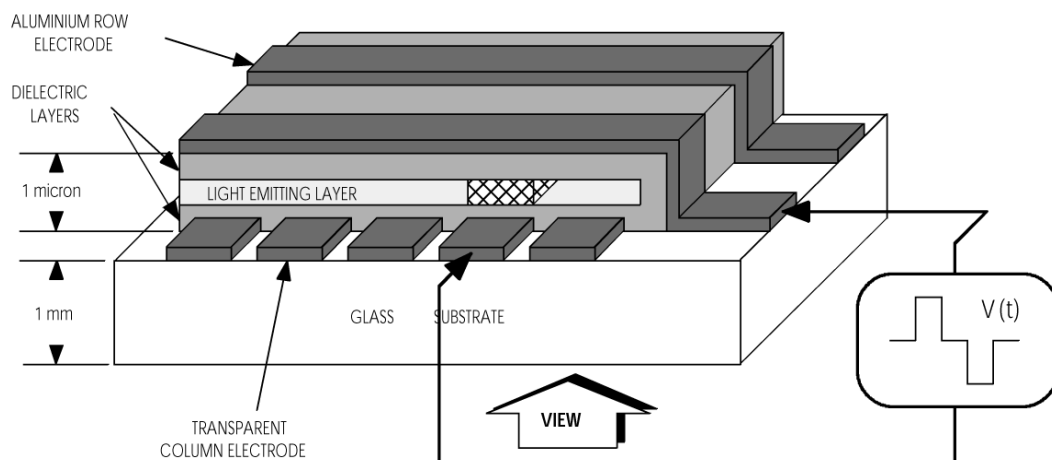


**Figure 1. TFEL technology**

The TFEL glass panel is a solid-state device with a thin film luminescent layer sandwiched between transparent dielectric layers and a matrix of row and column electrodes. The row electrodes, in back, are aluminum; the column electrodes, in front, are transparent. The entire thin film device is deposited on a single glass substrate. The glass panel is mounted to an electronic circuit assembly board (ECA) with an elastic spacer. The ECA is connected to the TFEL glass panel with flexible interconnects. The result is a flat, compact, reliable and rugged display device.

The EL640.400-CD4 display includes a dark ICEBrite™ (Integral Contrast Enhancement) background in the display glass. The ICEBrite background significantly improves the luminance contrast of the display in bright ambient. The ICEBrite also removes the halo around the lit pixels in dark ambient making the appearance of each pixel crisp and clear.

In the Beneq EL640.400-C displays, the 640 column electrodes and 400 row electrodes are arranged in an X-Y formation with the intersecting areas performing as pixels. Voltage is applied to both the correct row electrode and the correct column electrode to cause a lit pixel. Operating voltages required are provided by an integral DC/DC converter.

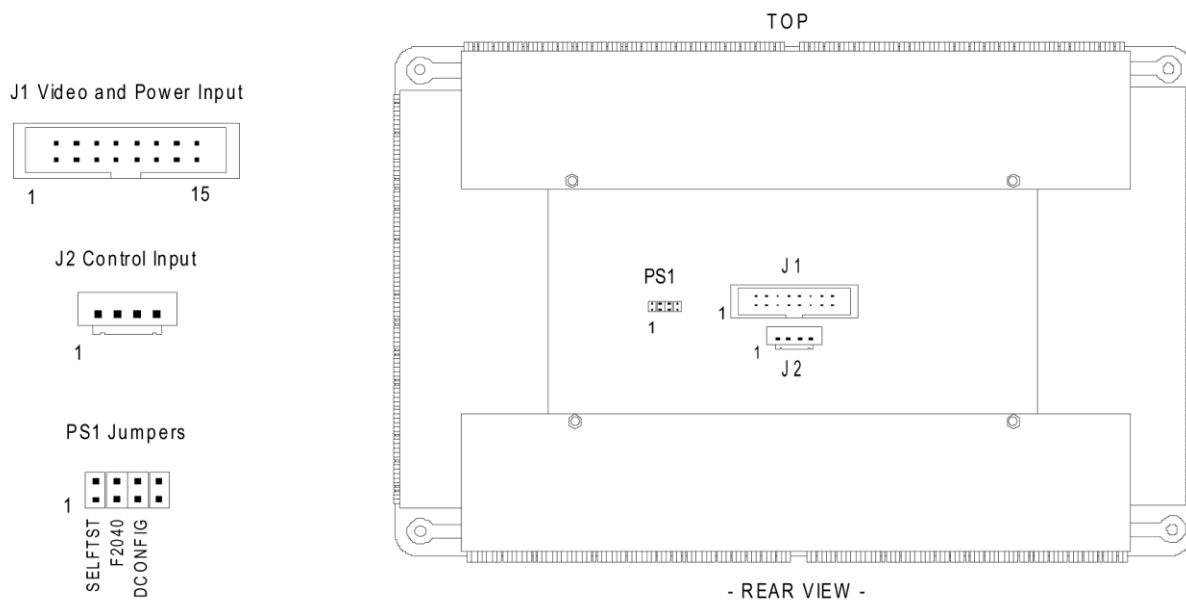# 3   Electrical characteristics

## 3.1   Connector layout

**Figure 2. Input connectors and their location**

## 3.2 Input to the display

**Table 1. Input to the display**

| Pin No. | Signal | Symbol | Description |
|---------|--------|--------|-------------|
| **J1(data and power input connector)** | | | |
| 1, 2 | Voltage | $V_{cc2}$ | Supply voltage (+12 V/+24 V dependent on version, see Ordering Information on page 23) converted to required internal high voltages. |
| 3, 4 | Voltage | $V_{cc1}$ | Supply voltage (+5 V) for the logic. |
| 5 | Blanking | _BLANK | Used in VGA modes. In NORMAL mode, should be pulled HIGH or left disconnected. |
| 6, 8, 10 12, 14, 16 | Ground | GND | Signal return. |
| 7 | Two-bit data | TVID | Second data input for two-bits-parallel mode. The TVID input is for odd columns and the VID for even columns. |
| 9 | Vertical Sync | VS | The vertical sync signal VS controls the vertical position of the picture. |
| 11 | Horizontal Sync | HS | The horizontal sync signal HS controls the internal row counter and in the NORMAL mode the horizontal position of the picture. |
| 13 | Video Clock | VCLK | The VCLK signal shifts data present on the VID and TVID lines into the display system. VCLK is active on the rising edge. |
| 15 | Video Data | VID | Signal that supplies the pixel information to the system. |
| **J2 (optional control input connector)** | | | |
| 1 | Luminance Pot.1 | LUMPOT1 | The inputs for an external logarithmic 50 kΩ potentiometer to adjust the luminance of the display. Can be left disconnected. The luminance is then at the maximum level. |
| 2 | Luminance Pot.2 | LUMPOT2 | |
| 3 | Enable | ENABLE | Display operation is enabled if HIGH or left disconnected. |
| 4 | Ground | GND | Same as pins 6…16 in J1 (not necessary to be connected). |

## 3.3   Control basics

The TFEL panel has 640 transparent column electrodes crossing 400 row electrodes in an X-Y fashion. Light is emitted when an AC voltage is applied at a row- column intersection. The display operation is based on the symmetric, line-at-a-time data addressing scheme, which is synchronized by the external VS, HS, and VCLK input signals. The internal control signals and the high voltage pulses for the column and row drivers are generated internally by the control electronics. All control signal inputs are HCT-compatible.

## 3.4   Power input

The required supply voltages for the display are +5 $V_{DC}$ ($V_{cc1}$) for the logic and either +12 $V_{DC}$ (-CB1 and -CD4) or +24 $V_{DC}$ (-CB3) ($V_{cc2}$) for the integrated DC/DC converter. The high voltages needed for driving the display are generated by the DC/DC converter from the $V_{cc2}$ input voltage.

## 3.5   Signal inputs

For easy interfacing with VGA display controllers, the data and control input signals are VGA Feature Connector compatible. The display automatically determines the mode of operation.

The control input J2 includes contacts for optional luminance control and the ENABLE signal to totally shut off the display when not in use (screensaver function).

## 3.6   Connectors

**Table 2. Connectors**

| J1 | 16-pin header | ODU 511.066.003.016 or eq. |
|----|---------------|----------------------------|
|    | Mating        | ODU 517.065.003.016 or eq. |
| J2 | 4-pin header  | Hirose DF1–4P–2.5DSA or eq. |
|    | Mating        | Hirose DF1–4S–2.5 R 28 or eq. |

## 3.7   Luminance control

The displays feature luminance control capability for users to set the brightness of the display to meet the ambient lightning. The control function is achieved by drawing a 0…1 mA current from LUMPOT1 to ground (LUMPOT2). The luminance is at the maximum level when the inputs are open. The voltage level of LUMPOT1 (J2/1) is approximately 5.1 $V_{DC}$ when disconnected.

## 3.8   Self-test

The operation of the display can be easily checked using the SELFTST function. Self-test is performed when the SELFTST jumper (PS1/1) is set or no data input is present. During self-test, all pixels are lit except the left-most half of the topmost row of the display.

**Beneq Products Oy**
Olarinluoma 9                          Tel. +358 9 7599 530                     VAT ID FI25115461
FI-02200 Espoo                         Fax +358 9 7599 5310                     www.beneq.com
Finland                                lumineq@beneq.com                        www.lumineq.com

Date: March 13, 2014                   Document number: ED000820A               Page | 7

## 3.9 Jumper description

**Table 3. PS1**

| Position name | Function |
|---|---|
| 1 SELFTST | Self-test function is selected, if the SELFTEST jumper is ON. In self-test, the input video data at VID and TVID inputs are displayed asynchronously without any other input signals. |
| 2 F2040 | 200 lines mode. All data is repeated in two consecutive rows. Normally should not be installed. |
| 3 DCONFIG | The two-bits-parallel mode is selected if this jumper is set (see page 10). |
| 4 | Reserved. |

When shipped from the factory, no jumpers are set.

## 3.10 Input specifications

**Table 4. Input specifications**

| Parameter | Symbol | Min. | Typ. | Max. | Absolute max. rating |
|---|---|---|---|---|---|
| Logic input HIGH | | 2 V | | | $V_{cc1}$ + 0.5 V |
| Logic input LOW | | | | 0.8 V | −0.5 V |
| Logic supply voltage | $V_{cc1}$ | 4.75 V | 5.0 V | 5.25 V | 6 V |
| Logic supply current at 5 V | $I_{cc1}$ | — | — | 0.2 A | |
| Display Supply voltage (CB1, CD4) | $V_{cc2}$ | 10.8 V | 12 V | 14.4 V | 15 V |
| (CB3) | $V_{cc2}$ | 21.6 | 24 V | 26.4 V | 30 V |
| Supply current at +12 V (CB1, CD4) | $I_{cc2}$ | — | 0.8 A | 1.5 A | |
| Supply current at +24 V (CB3) | $I_{cc2}$ | — | 0.5 A | 0.8 A | |
| Power consumption 5 V & 12 V | | — | 11 W | 19 W | |
| Power consumption 5 V & 24 V | | — | 13 W | 20 W | |

Operating conditions: Frame rate 70 Hz, ambient temperature 25 °C.

**NOTE:** Absolute maximum ratings are those values beyond which damage to the device may occur. The minimum and maximum specifications in this Operation Manual should be met, without exception, to ensure the long-term reliability of the display. Beneq does not recommend operation of the display outside these specifications.

**Beneq Products Oy**
Olarinluoma 9
FI-02200 Espoo
Finland

Tel. +358 9 7599 530
Fax +358 9 7599 5310
lumineq@beneq.com

VAT ID FI25115461
www.beneq.com
www.lumineq.com

Date: March 13, 2014                    Document number: ED000820A                    Page | 8

# 4  Display features

## 4.1  Display operation modes

The displays have two input timing modes. The VGA mode supports standard 200, 350 and 400 row VGA modes and the normal mode is similar to the normal mode in most Beneq displays. The operation mode is determined from a combination of the polarities of the VS and HS pulses and the _BLANK signal at the rising edge of the VS pulse and the polarities of VS and HS pulses at the rising edge of the _BLANK pulse.

In the VGA modes, the number of columns is determined by the number of VCLK pulses during a HS pulse. A tolerance of ±1 pulse is accepted.

**VGA modes:** The display data and control input is compatible with feature connector signals from VGA board. The display supports VGA modes 0, 1, 2, 3, 0*, 1*, 2*, 3*, 0+, 1+, 2+, 3+, 4, 5, 6, 7, 7+, D, E, F, 10 and 13. It notifies the polarity of the HS and VS at the rising edge of BLANK and determines the number of rows in the mode.

**Note that in VGA modes 0, 1, 0*, 1*, 0+, 1+, 4, 5, D and 13 where the software uses 320 or 360 columns, the size of borders varies from one VGA controller to another. Therefore, the image may not be centered properly using those modes.**

The image is centered automatically, and in text modes with 720 pixels horizontally, every ninth pixel is omitted for compatibility. The non-displayed pixel is in the space region of the character matrix, and therefore no information is lost. The borders are normally eliminated because of the centering. The upper and lower borders are, however, displayed in the modes using 350 rows due to extra rows not needed for the picture.

The 480 row VGA modes are not supported. Even if the display does not scan in these modes (11, 12), it continues to operate with no failures when a supported mode is detected.

**Normal mode:** This mode is pin and timing compatible with the MD640.400 Series displays and the normal mode of the EL640.400-C3/CD3 series displays. In this mode, only four input signals are needed: video data (VID), video clock (VCLK), horizontal synchronizing (HS) and vertical synchronizing (VS). _BLANK is not in use and should be pulled high or left disconnected.

In the normal mode, the last 640 pixels before the fall of the HS are displayed. The topmost row displayed is the first HS HIGH time ending after HS Hold from VS time (T4 in normal mode) from the rising edge of VS. If HS is running continuously, the rising edge of the VS can be simultaneous to the previous falling or rising edge of the HS. See details on setup and hold timing as well as normal mode timing on page 14.

**Beneq Products Oy**
Olarinluoma 9
FI-02200 Espoo
Finland

Tel. +358 9 7599 530
Fax +358 9 7599 5310
lumineq@beneq.com

VAT ID FI25115461
www.beneq.com
www.lumineq.com

Date: March 13, 2014              Document number: ED000820A              Page | 9

## 4.2 Supported VGA modes

**Table 5 Supported VGA modes**

| VGA mode | Type | Text format | Char. box | Vsync freq. (Hz) | Pixels (software) | Double Scan | Border size H | V |
|---|---|---|---|---|---|---|---|---|
| 0, 1 | text | 40 x 25 | 8 x 8 | 70 | 320 x 200 | Yes | 0 | 7 |
| 2, 3 | text | 80 x 25 | 8 x 8 | 70 | 640 x 200 | Yes | 8 | 7 |
| 0*, 1* | text | 40 x 25 | 8 x 14 | 70 | 320 x 350 | No | 0 | 6 |
| 2*, 3* | text | 80 x 25 | 8 x 14 | 70 | 640 x 350 | No | 8 | 6 |
| 0+, 1+ | text | 40 x 25 | 9 x 16 | 70 | 360 x 400 | No | 0 | 7 |
| 2+, 3+ | text | 80 x 25 | 9 x 16 | 70 | 720 x 400 | No | 9 | 7 |
| 4, 5 | graph | 40 x 25 | 8 x 8 | 70 | 320 x 200 | Yes | 0 | 7 |
| 6 | graph | 80 x 25 | 8 x 8 | 70 | 640 x 200 | Yes | 8 | 7 |
| 7 | text | 80 x 25 | 9 x 14 | 70 | 720 x 350 | No | 9 | 6 |
| 7+ | text | 80 x 25 | 9 x 16 | 70 | 720 x 400 | No | 9 | 7 |
| D | graph | 40 x 25 | 8 x 8 | 70 | 320 x 200 | Yes | 0 | 7 |
| E | graph | 80 x 25 | 8 x 8 | 70 | 640 x 200 | Yes | 8 | 7 |
| F | graph | 80 x 25 | 8 x 14 | 70 | 640 x 350 | No | 8 | 6 |
| 10 | graph | 80 x 25 | 8 x 14 | 70 | 640 x 350 | No | 8 | 6 |
| 13 | graph | 40 x 25 | 8 x 8 | 70 | 320 x 200 | Yes | 0 | 7 |
| Normal mode | graphics | | | 72 max | 640 x 400 | | | |

NOTES:

In VGA modes 0+, 1+, 2+, 3+, 7 and 7+, the character box width is narrowed to 8 pixels by omitting the data of every 9th pixel. In VGA modes 0, 1, 0*, 0+, 1+, 4, 5, D and 13 where the software uses 320 or 360 columns, the size of borders may vary from one VGA controller card to another. The potentially needed picture adjustments may be done by programming the registers of the VGA controller chip.

Double Scan is a VGA card feature.

VGA modes 11 and 12 with 480 rows are not supported.

## 4.3 Display enable

The display can be totally shut off for screen save or power reduction by a LOW sate in the ENABLE control input. When disabled, the display is totally dark and only the DC/DC converter remains functional consuming only approximately 2 W. In normal operation, the ENABLE input should be pulled HIGH or left disconnected (internal pull-up).

## 4.4 200 rows mode

200 input data rows may be displayed using 400 rows by automatically doubling every data row to two consecutive display rows. This function is selected by installing the jumper PS1/2 (F2040). The _BLANK input must also be in LOW state. For more information of this mode, contact Beneq.

## 4.5 Two-bits-parallel data

To reduce the input data frequency in the normal mode, the video data can be input two bits per clock cycle. The two data inputs are organized so that the data for the odd columns, numbered from left to the right at the viewer side, is input at the TVID (J1/ pin 7) and the data for the even columns at VID (J1/ pin 15). The two-bits-parallel mode is selected by installing the jumper 3 of the pin stripe PS1.

## 4.6 Brightness control

The brightness of the display can be adjusted (approximately between 10% and 100%) by an external 50 logarithmic potentiometer between the LUMPOT1 and LUMPOT 2 inputs (J2/pins 1 and 2). The control function is done by feeding a small DC current signal via the external potentiometer from LUMPOT1 (+5 V reference voltage) to LUMPOT2. If the two inputs are left disconnected, the brightness is at its maximum level.

## 4.7 Self-test

The operation of the display can be easily checked without any external signals using the self-test function.

- Insert the jumper 1 in the pin stripe PS2.
- Connect power to the display.

All the pixels of the display will be lit with the exception of the first half of the topmost row.

# 5 Installation and handling

## 5.1 Mounting

Mounting of the display should be done using the M3 insert nuts on the four corners of the plastic assembly support or the four holes in the FRA frames.

Note that because all four mounting points are internally connected to signal ground, care should be taken to avoid grounding loops.

## 5.2 Handling

Before handling the display, necessary precaution must be taken to prevent application of static charges on the display from the operator or tools.

The display is made of glass material and should be handled with proper care. Do not drop the display or allow hard objects to strike its surface.

The flexible interconnects between the display glass and the ECA carry high voltages and are very sensitive to touch. Handling and mounting of the display should be done from the four corners of the assembly support only.

## 5.3 Cable length

For trouble-free data transfer from data transmitter to display input connector, a maximum cable length of 600 mm (24 in.) is recommended. In case of VGA feature connector use, proper signal buffering should be ensured. In order to lower signal reflections, the connecting cable should be terminated with approximately 100 series resistor at each of the five signal line outputs of the signal source.

## 5.4 Avoiding burn-in

As with any other light-emitting display, luminance variations may be noticed if fixed patterns are displayed on the screen for extended periods. It is prudent to use a screensaver or image inversion to avoid burn-in.

**ELECTROSTATIC CAUTION:** This Beneq display uses CMOS and power MOS-FET devices. These components are electrostatic-sensitive. Unpack, assemble and examine this assembly in a static controlled area only. When shipping, use packing materials designed for protection of electrostatic-sensitive components.

**WARNING:** The product generates potentially dangerous voltages capable of causing personal injury (high voltage pulses up to 195 $V_{AC}$). Do not touch the display electronics during operation!
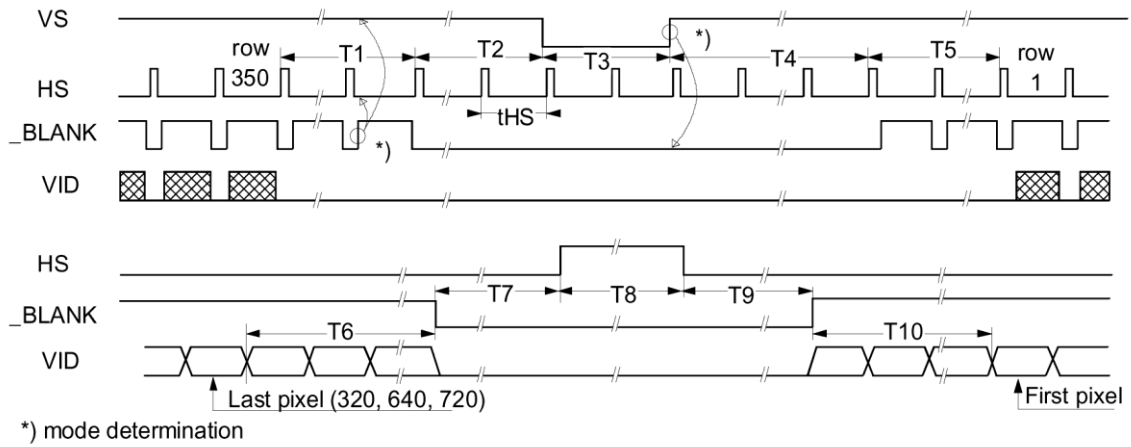
## 5.5 Timing characteristics



*) mode determination

**Figure 3. Row VGA modes (see page 9)**

**Table 6. 350 row VGA modes**

| Description | | | Unit |
|---|---|---|---|
| T1 Vertical Border | 6 | | tHS |
| T2 Vertical Front Porch | 31 | | tHS |
| T3 VS Pulse Width | 2 | | tHS |
| T4 Vertical Back Porch | 54 | | tHS |
| T5 Vertical Border | 6 | | tHS |
| HS pulses / VS | 449 | | |
| VS frequency | 70 | | Hz |

| Description | 320 | 640 | 720 | Unit |
|---|---|---|---|---|
| T6 Horizontal Border | 0 | 8 | 9 | tVCLK |
| T7 Horizontal Front Porch | 8 | 8 | 9 | tVCLK |
| T8 HS Pulse Width | 48 | 96 | 108 | tVCLK |
| T9 Horizontal Back Porch | 24 | 40 | 45 | tVCLK |
| T10 Horizontal Border | 0 | 8 | 9 | tVCLK |
| VCLK pulses / HS | 400 | 800 | 900 | |
| HS period | 31.8 | 31.8 | 31.8 | µs |
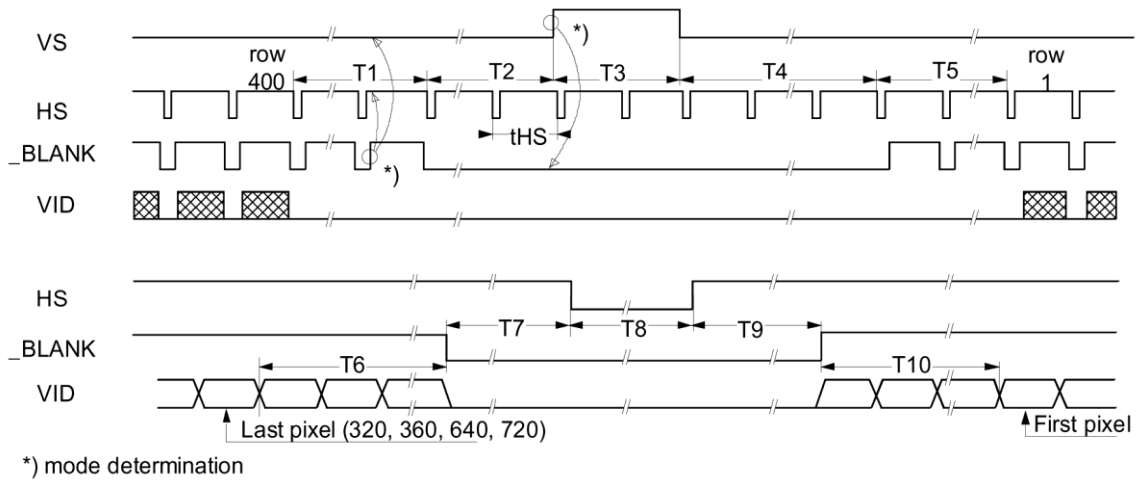
**Figure 4. 400 row VGA modes (see page 9)**

**Table 7. 400 row VGA modes**

| Description | | | | | Unit |
|---|---|---|---|---|---|
| T1 Vertical Border | | 7 | | | tHS |
| T2 Vertical Front Porch | | 5 | | | tHS |
| T3 VS Pulse Width | | 2 | | | tHS |
| T4 Vertical Back Porch | | 28 | | | tHS |
| T5 Vertical Border | | 7 | | | tHS |
| HS pulses / VS | | 449 | | | |
| VS frequency | | 70 | | | Hz |
| **Description** | **320** | **360** | **640** | **720** | **Unit** |
| T6 Horizontal Border | 0 | 0 | 8 | 9 | tVCLK |
| T7 Horizontal Front Porch | 8 | 9 | 8 | 9 | tVCLK |
| T8 HS Pulse Width | 48 | 54 | 96 | 108 | tVCLK |
| T9 Horizontal Back Porch | 24 | 27 | 40 | 45 | tVCLK |
| T10 Horizontal Border | 0 | 0 | 8 | 9 | tVCLK |
| VCLK pulses / HS | 400 | 450 | 800 | 900 | |
| HS period | 31.8 | 31.8 | 31.8 | 31.8 | µs |
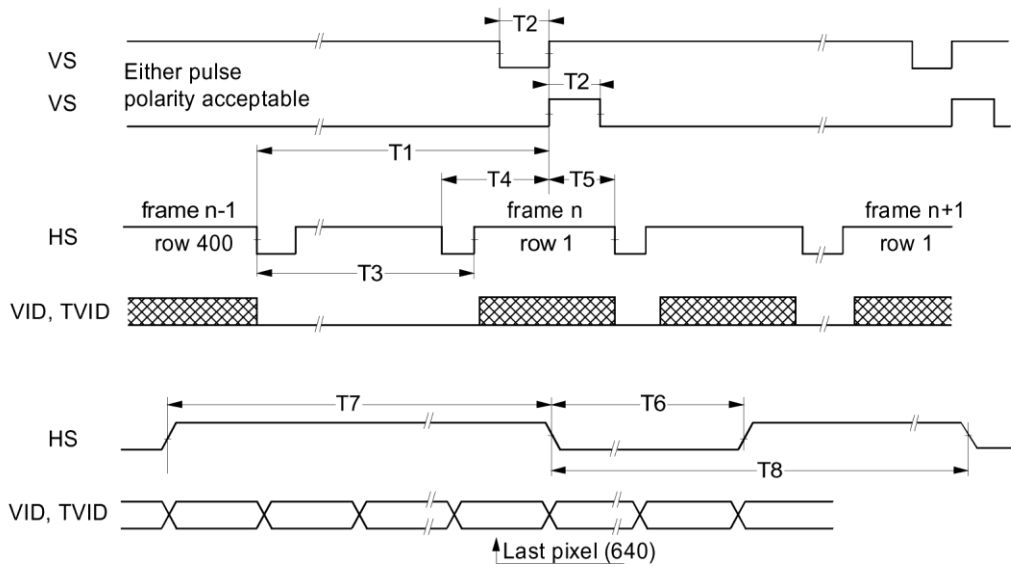
**Figure 5. 640 columns x 400 rows normal mode**

**Table 8. 640 columns x 400 rows normal mode**

| Description | Min | typ | Max | Unit |
|---|---|---|---|---|
| T1 Vertical Front Porch [1] | 60 | | | µs |
| T2 VS HIGH/LOW time [2] | 1 | | | tVCLK |
| T3 Vertical Blank | 40 | | | µs |
| VS frequency | | 70 | 72 | Hz |
| VS period | 400 | | | tHS |
| **Description** | **Min** | **Typ** | **Unit** | |
| T4 HS setup to VS | 9 | | tVCLK | |
| T5 HS hold from VS | 2 | | µs | |
| T6 HS Low Time [5] | 4 | | tVCLK | |
| T7 HS High Time [6] | 640 | 640 | tVCLK | |
| T8 HS period (tHS) | 31 | | µs | |

NOTES:

1) This is the time needed to display the last row and to change the frame.

2) Only rising edge is used.

5) Video Clock VCLK should be kept running continuously.

6) The number of VCLK pulses during HS high time should be even.
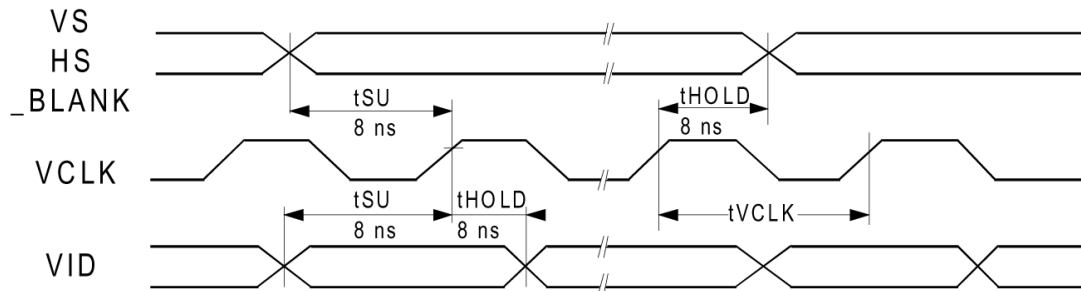
## 5.6    Setup and hold timing



**Figure 6. Setup and hold timing**

**Table 9. Setup and hold timing**

| Mode | tVCLK ns | fVCLK MHz |
|---|---|---|
| 2+, 3+, 7, 7+ | 35.31 | 28.322 |
| 2, 3, 2*, 3*, 6, E, F, 10 | 39.71 | 25.175 |
| 0+, 1+ | 70.62 | 14.161 |
| 0, 1, 0*, 1*, 4, 5, D, 13 | 79.43 | 12.588 |
| NORMAL | Min 33 | Max 30 |

# 6 Operational specifications

## 6.1 Environmental

**Table 10. Environmental characteristics**

| Temperature | |
|---|---|
| Operating | 0 °C …+55 °C |
| Non-operating | −40 °C …+85 °C |
| Operating survival | −20 °C …+65 °C (no permanent damage) |
| Test duration 24 h at -20 °C (without condensation) | |
| **Humidity** | |
| Relative humidity | +40 °C, 93% RH, operating (IEC 68-2-3) |
| Damp heat | +25 °C …+55 °C, 95% RH, non-operative (IEC 68-2-30) |
| **Altitude** | |
| Operative | 15,000 m (50,000 ft.) above sea level |
| **Vibration** | |
| | 20…500 Hz, ASD level 0.05 $G^2$/Hz, Random vibration wide band, IEC 68–2–36, Test Fdb |
| **Shock** | |
| Magnitude | 100 G |
| Duration | 4 ms (half sine wave) |
| Number of shocks | 18 (3 on each of the 6 surfaces), IEC 68-2-27, test Ea |

## 6.2 Reliability

MTBF >50 000 h @ 25 °C

## 6.3 Safety

The display will not inhibit the end product from obtaining any of the following specification:
UL1950, UL544, CSA154, IEC950

## 6.4 EMC

The display will not inhibit the end product from obtaining any of the following specifications:
EN55022 Class B, FCC Part 15J Class B

**Beneq Products Oy**
Olarinluoma 9
FI-02200 Espoo
Finland

Tel. +358 9 7599 530
Fax +358 9 7599 5310
lumineq@beneq.com

VAT ID FI25115461
www.beneq.com
www.lumineq.com

Date: March 13, 2014                    Document number: ED000820A                    Page | 17

## 6.5 Optical

Determined at 70 Hz frame rate at 25 °C

### 6.5.1 Display colour

Wide band amber (Zn:Mn)

**Table 11. Optical characteristics**

| Areal luminance | | |
|---|---|---|
| On luminance (typ) | CB1/CB3 | 53 cd/m$^2$ (16 fL) |
| | CD4 | 22 cd/m$^2$ (6.4 fL) |
| On luminance (min.) | CB1/CB3 | 45 cd/m$^2$ (13 fL) |
| | CD4 | 17 cd/m$^2$ (5.0 fL) |
| Measured at the center and the four corners of the screen. | | |
| **Non-uniformity** | | |
| | 35% | = (1− min. luminance/max luminance) x 100. Maximum difference between any two of five points (center and four corners) |
| **Luminance variation (time)** | | |
| Maximum | 20% | 10,000 h |
| **Luminance variation (temperature)** | | |
| Typical | 10% | Over the 0 °C …+55 °C range. |
| Maximum | 15% | |
| **Luminance contrast ratio** | | |
| Minimum | CD4 | 7:1 @500 lx<br>3:1 @ 1,800 lx |
| **Viewing angle** | | |
| Minimum | 160° | |

| Illuminance | Classification |
|---|---|
| 1 … 10 lx | Dark |
| 10 … 100 lx | Dim |
| 100 … 1,000 lx | Office |
| 1,000 … 10,000 lx | Bright |
| 10,000 … 100,000 lx | Sunlight |

### 6.5.2 Filter

The luminance contrast of the ICE display CD4 is sufficient for operation without contrast enhancement filter. For the best overall performance of the monochrome CB1 and CB3 displays in high or low ambient light levels, a neutral gray circular polarizing filter with anti-reflective coating or etch is recommended. This filter will make the background of the display darker and improve the luminance contrast ratio. The anti-reflective coating on the filter should face the user.

## 7   Mechanical characteristics

### 7.1   Display external dimensions

Figure 7 shows the mechanical dimensions of a standard EL640.400−CB1 /CB3 or −CD4 display unit. The display can also be delivered with aluminium mounting frames (see Figure 9). See Ordering Information on page 23.

**Table 12. Display external dimensions**

| Height | 147 mm | 5.79 in. |
|---|---|---|
| Width | 225 mm | 8.86 in. |
| Depth | 23 mm | 0.91 in. |
| Weight | 400 g | 14 oz. |

### 7.2   Display viewing area characteristics

**Table 13. Display viewing area characteristics**

| Active area | | |
|---|---|---|
| millimeters (inches) | height | 121.8 (4.80) |
| | width | 195.0 (7.68) |
| **Pixel pitch** | | |
| millimeters (inches) | height | 0.305 (0.012) |
| | width | 0.305 (0.012) |
| **Pixel size** | | |
| millimeters (inches) | height | 0.178 (0.007) |
| | width | 0.212 (0.008) |
| **Pixel fill factor** | 41% | |
| **Pixel matrix** | 640 horizontal by 400 vertical | |

**CAUTION:** The ambient temperature of the display should not be allowed to exceed the environmental specifications (see Table 10). In most applications, an air gap of

approximately 5 mm is recommended (see mechanical drawings). Some applications may require, however, a larger air gap or cooling of the display unit in the system. Note that this may slightly increase the total depth of the design.
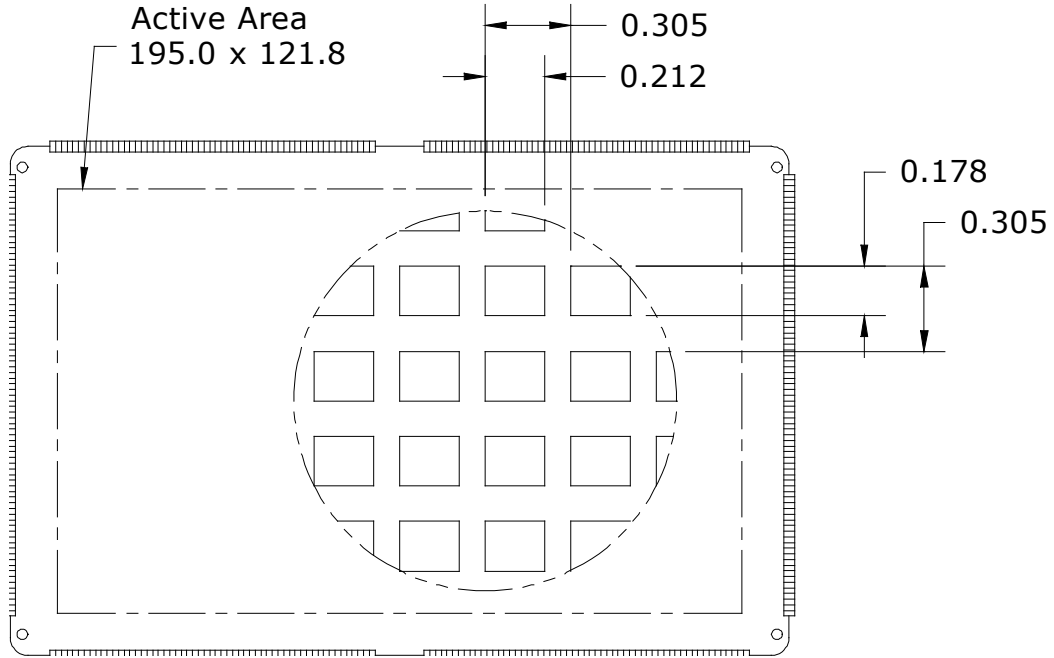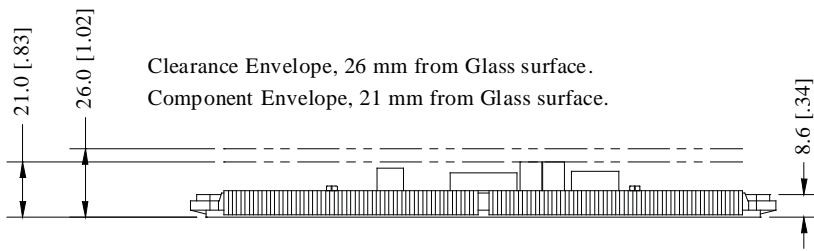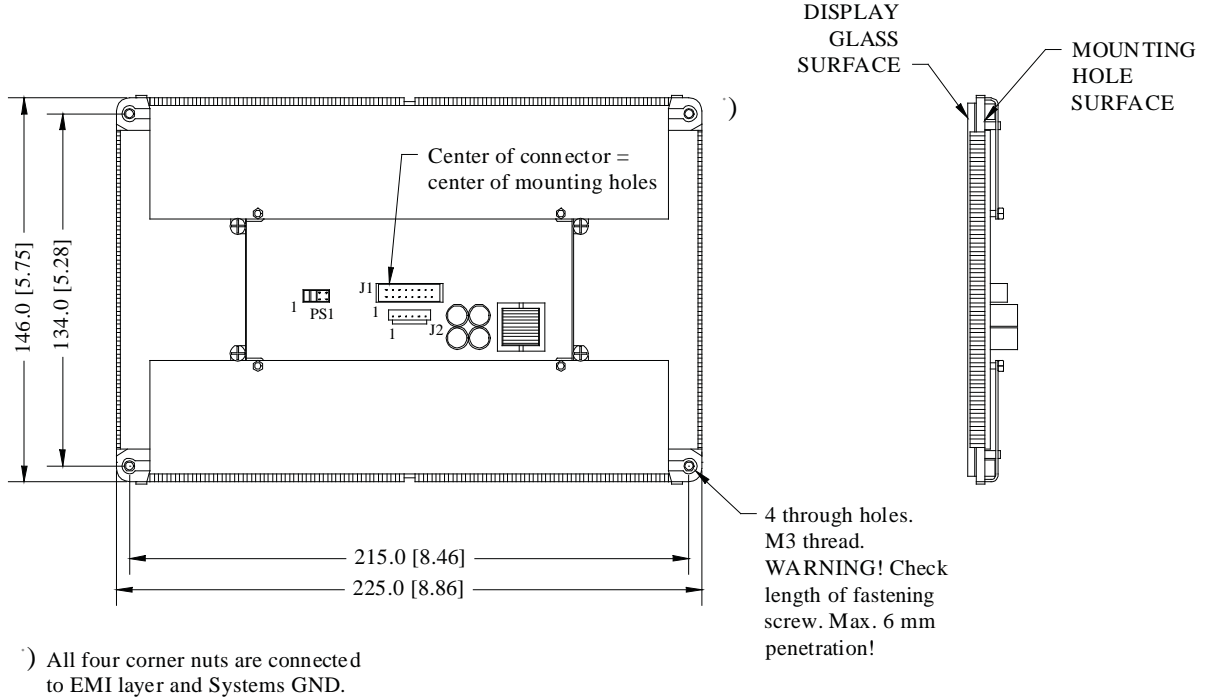


**Figure 7. Viewing area characteristics**

Clearance Envelope, 26 mm from Glass surface.
Component Envelope, 21 mm from Glass surface.

21.0 [.83]
26.0 [1.02]
8.6 [.34]

| TOLERANCES: (unless otherwise specified) | |
| --- | --- |
| 0 ... 6 mm | ± 0.1 mm |
| 6 ... 30 mm | ± 0.2 mm |
| 30 ... 120 mm | ± 0.3 mm |
| 120 ... 320 mm | ± 0.5 mm |
| angular | ± 2° |

DISPLAY GLASS SURFACE

MOUNTING HOLE SURFACE

Center of connector = center of mounting holes

146.0 [5.75]
134.0 [5.28]

1 PS1
J1
1
1
J2

215.0 [8.46]
225.0 [8.86]

4 through holes. M3 thread. WARNING! Check length of fastening screw. Max. 6 mm penetration!

') All four corner nuts are connected to EMI layer and Systems GND.

Dimensions in mm (inches).

**Figure 8. EL640.400-CB1/CB3 and -CD4 back and side views**

26.0 [1.02]
21.0±0.4 [.83±.02]
17.0 [.67]

Clearance Envelope, 26mm from Glass surface.
Component Envelope, 21mm from Glass surface.

| TOLERANCES: (unless otherwise specified) | |
|---|---|
| 0 ... 6 mm | ± 0.1 mm |
| 6 ... 30 mm | ± 0.2 mm |
| 30 ... 120 mm | ± 0.3 mm |
| 120 ... 320 mm | ± 0.5 mm |
| angular | ± 2° |

Center of connector = center of mounting holes

158.5 [6.24]
116.0 [4.57]

1 PS1
J1
1
1 J2

1.5 [.06]
2.2 [.09]

Display Glass Surface

Mounting Hole Surface

140.4 [5.53]
142.5 [5.61]

11.3 [.44]

220.5 [8.68]
228.5 [9.00]

*) The frame is connected to GND.     Dimensions in mm (inches).

4 through holes. M3 thread. WARNING! Check length of fastening screw. Max. 4 mm penetration!

**Figure 9. EL640.400-CB1/CB3 and −CD4 FRA back and side views**

# 8  Description of warranty

Seller warrants that the Goods will conform to published specifications and be free from defects in material during warranty time from delivery. To the extent that goods incorporate third-party-owned software, seller shall pass on seller's licensor's warranty to buyer subject to the terms and conditions of seller's license.

Warranty repairs shall be warranted for the remainder of the original warranty period. Buyer shall report defect claims in writing to seller immediately upon discovery, and in any event, within the warranty period.  Buyer must return goods to seller within 30 days of seller's receipt of a warranty claim notice and only after receiving seller's return goods authorization. Seller shall, at its sole option, repair or replace the goods.

If goods were repaired, altered or modified by persons other than seller, this warranty is void. Conditions resulting from normal wear and tear and buyer's failure to properly store, install, operate, handle or maintain the goods are not within this warranty. Repair or replacement of goods is seller's sole obligation and buyer's exclusive remedy for all claims of defects.  If that remedy is adjudicated insufficient, Seller shall refund buyer's paid price for the goods and have no other liability to buyer.

All warranty repairs must be performed at seller's authorized service center using parts approved by seller. Buyer shall pay costs of sending goods to seller on a warranty claim and seller shall pay costs of returning goods to buyer. The turnaround time on repairs will usually be 30 working days or less. Seller accepts no added liability for additional days for repair or replacement.

If seller offers technical support relating to the goods, such support shall neither modify the warranty nor create an obligation of seller. Buyer is not relying on seller's skill or judgment to select goods for buyer's purposes.  Seller's software, if included with goods, is sold as is, and this warranty is inapplicable to such software.

SELLER DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

# 9  Easy to use

There are many options available, which make Beneq flat panel displays easy to use, easy to interface, and easy to package. Examples of options typically available include filters, touch panels and interface cards. Call Beneq for complete information and availability.

**Beneq Products Oy**
Olarinluoma 9
FI-02200 Espoo
Finland

Tel. +358 9 7599 530
Fax +358 9 7599 5310
lumineq@beneq.com

VAT ID FI25115461
www.beneq.com
www.lumineq.com

Date: March 13, 2014                  Document number: ED000820A                  Page | 23

# 10 Ordering information

| Product | Part number | Description |
|---|---|---|
| EL640.400–CB1 | 996-5072-00LF | EL640.400 non-ICE, operating temperature 0 ºC - +55 ºC. |
| EL640.400–CB1 FRA | 996-5073-00LF | EL640.400 non-ICE, operating temperature 0 ºC - +55 ºC, with an aluminum mounting frame |
| EL640.400–CB3 FRA | 996-5078-00LF | EL640.400-CB series display with a $V_H$ of 24 V nominal input and frame. |
| EL640.400–CD4 FRA | 996-5085-00LF | EL640.400 ICE, otherwise same as EL640.400 CB1-FRA |

# 11 Support and service

Beneq Products is a Finnish company based in Espoo, Finland, with a world-wide sales distribution network. Full application engineering support and service are available to make the integration of Lumineq displays as simple and quick as possible for our customers.

**RMA Procedure:** For a Returned Material Authorization number, please contact Beneq Products Oy by email (rma.lumineq@beneq.com) with the model number(s), serial number(s) and brief description of the problem. When returning goods for repair, please include a brief description of the problem, and mark the outside of the shipping container with the RMA number.

# 12 RoHS II

Beneq Products OY is committed to continuous improvement. As part of this process we are fully in support of EU directive 2011/65/EU, the Restriction of Hazardous Substances, commonly known as RoHS II or RoHS Recast, which, compared to RoHS, keeps the restrictions on the original six hazardous substances, including lead (Pb) in electronic equipment. It also expands these restrictions to previously exempted categories including medical devices and monitoring and control instruments.

Beneq part number with an "LF" suffix designation indicates RoHS compliance, as shown on the part number label affixed to the display and on the box containing the display.