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SHARP

Specification

Note: This specification is subject to change without prior notice

АКТИВНЫЙ КОМПОНЕНТ ВАШЕГО БИЗНЕСА

Тел.: (495) 232-2522 • факс: (495) 234-0640 • info@prochip.ru • www.prochip.ru

Application Information for Sharp's LQ104V1LG81 LCD

Sharp Microelectronics of the Americas

INTRODUCTION

This Application Note provides additional design assistance for Sharp's LQ104V1LG81 LCD. This module is a landscape-mode, transmissive, active-matrix VGA liquid crystal module with very wide viewing angles, high brightness and very high contrast. It is a True Industrial panel, meeting Sharp's criteria for Strong 2 panels, with extended temperature operation, shock and vibration resistance, a 50,000-hour-rated backlight; and utilizes a Low Voltage Differential Signalling (LVDS) interface for simple integration.

Subjects covered will be:

- Mechanical Specifications, including dimension drawings and connector specifications
- Absolute Maximum Ratings
- Optical Specifications, including view angles, reflectivity, contrast, and risetime
- Electrical Characteristics, including interfacing and signal timing information
- Design Notes
- Manufacturing Information, including handling and storage
- Reliability Information

This Information is based on Sharp's document number LD-22X52A and is designed to provide supplementary information for the Specifications for this part.

Always refer to the latest Specifications when designing with these devices.



FEATURES

- Landscape-mode, normally-white, transmissive thin-film-transistor (TFT) color panel (262 k colors)
- VGA Resolution (640 × 480)
- 450 nits brightness and 800:1 contrast
- 50,000-hr rated backlight
- Wide viewing angles: horizontal: 160°, vertical: 145°
- LVDS interface
- Built-in PWM backlight driver
- RoHS compliant

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATION	UNIT
Screen Size	10.4	Inch
Viewing Area	211.2 (H) × 158.4 (V)	mm
Dot Configuration (Square panel)	640 (H) × 480 (V)	Dots
Pixel Pitch	0.33 (H) × 0.33 (V)	mm
Pixel Array	RGB Vertical Stripe	
External Dimensions	246.5 (W) × 179.4 (H) × 12.5 (D)	mm
Display Mode	Normally White	
Mass	—	g

Connector Specifications

Table 1. Input Terminals and Functions

NO.	SYMBOL	FUNCTION	NOTES
1	Vcc	+3.3 V supply	
2	Vcc	+3.3 V supply	
3	GND		
4	GND		
5	RXIN0-	LVDS CH0 negative differential data input	
6	RXIN0+	LVDS CH0 positive differential data input	
7	GND		
8	RXIN1-	LVDS CH1 negative differential data input	
9	RXIN1+	LVDS CH1 positive differential data input	
10	GND		
11	RXIN2-	LVDS CH2 negative differential data input	
12	RXIN2+	LVDS CH2 positive differential data input	
13	GND		
14	RXCLK IN-	LVDS negative differential clock input	
15	RXCLK IN+	LVDS positive differential clock input	
16	GND		
17	NC		1
18	SCAN	Horizontal/Vertical display mode select	2
19	GND		
20	GND		

NOTES:

- Horizontal start timing is set by ENAB rise. When ENAB is tied LOW, horizontal start timing is as in *Input Timing Characteristics*. Never tie ENAB HIGH when the module is operating.
- See Figure 1: Scan State Results
- Mating connector: FI-SE20M or FI-S20S (JAE)

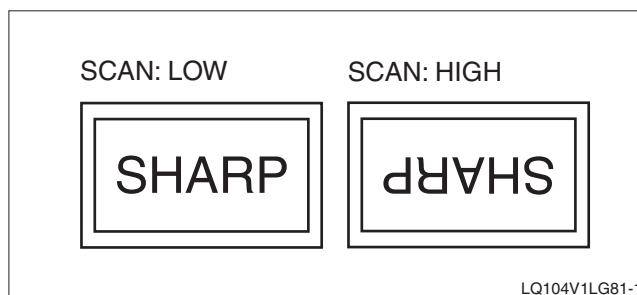


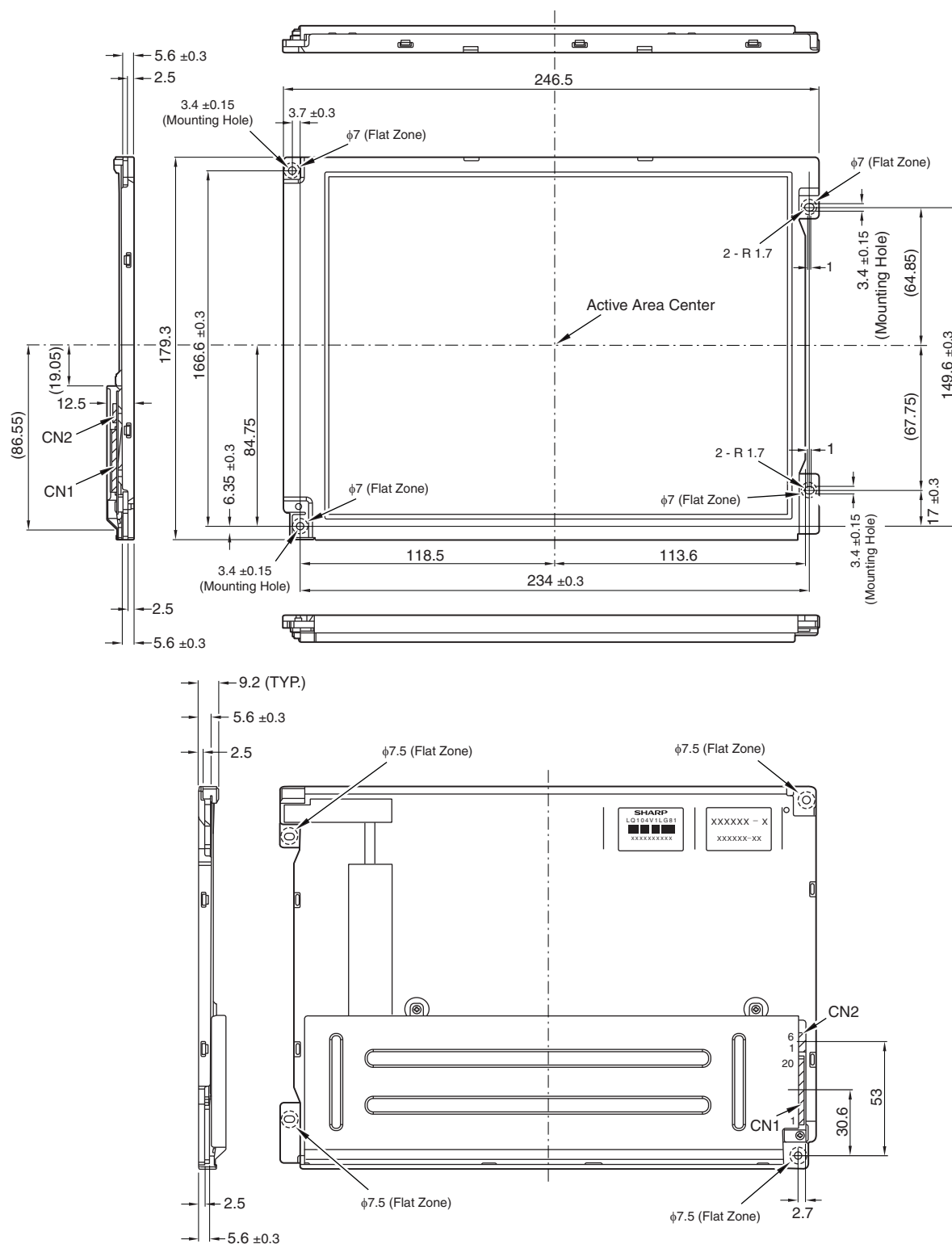
Figure 1. SCAN State Result

Table 2. LED Backlight Connector

PIN	SYMBOL	FUNCTION
1	Vdd	+12 V supply
2	Vdd	+12 V supply
3	GND	GND
4	GND	GND
5	XSTABY	Backlight ON/OFF signal
6	VBR	PWM signal

NOTE: Mating connector: SHLP-06V-S-B J.S.T. Mfg. Co. Ltd.

Mechanical Dimensions



NOTES:

- NOTES:
1. Bezel Opening: 214.6 × 162.4
 2. Active Area: 211.2 × 158.4
 3. Units: mm

LQ104V1LG81-23

Absolute Maximum Ratings

Ta = 25°C

PARAMETER	SYMBOL	PIN	MIN.	MAX.	UNIT	NOTES
Supply Voltage	Vcc	Vcc	-0.3	+4.0	V	2
	Vdd	Vdd	-0.3	+15.0	V	
Input Voltage	V _{I1}	Rx IN -/+ CK IN -/+	-0.3	Vcc + 0.3	V	
	V _{I2}	SCAN	-0.3	Vcc + 0.3	V	
	V _{I4}	XSTABY VBR	-0.3	Vdd	V	
Storage Temperature	Tstg		-30	+80	°C	
Operating Temperature	Topr		-30	+80	°C	

NOTES:

- Humidity 95% MAX. or less (Ta > 40°C). Maximum wet bulb temperature is 39°C or lower. No condensation is allowed.
- Vcc must be rated for 3 A.
- Deterioration in image quality may occur at temperatures from 65°C to 80°C, even though the LC module will not fail.
- Minimum temperature figure given is ambient.

OPTICAL SPECIFICATIONS

Vcc = +3.3 V, Ta = 25°C

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Viewing Angle	H	θ21, θ22	(70)	(80)	-	° (degrees)	1
	V	θ11	(45)	(65)	-	° (degrees)	1
		θ12	(70)	(80)	-	° (degrees)	1
Contrast Ratio		CR	(450)	(800)	-		2
Response Time	White/Black	τr + τf		(35)		ms	3
Chromaticity	White	x	(0.250)	(0.300)	(0.350)		
		y	(0.270)	(0.320)	(0.370)		
Chromaticity	Red	x	-	(0.560)	-		
		y	-	(0.325)	-		
Chromaticity	Green	x	-	(0.335)	-		
		y	-	(0.595)	-		
Chromaticity	Blue	x	-	(0.155)	-		
		y	-	(0.120)	-		
Luminance	White	Y _{L1}	(360)	(450)	-	nits	
Uniformity	White		-	-	(1.33)		

NOTES:

- Viewing Angle is described as clock positions: θ12 = 12 o'clock, θ11 = 6 o'clock, θ21 = 3 o'clock, θ22 = 9 o'clock. See Figure 5 for measurement methods.
- Contrast Ratio = luminance with all pixels white, divided by the luminance with all pixels black.
- Response Time is measured by the change interval in an optical receiver when the test panel's signal is transitioned from black to white to black. See Figure 6 for the measurement setup and Figure 3 for the output waveshape.
- White Uniformity is defined as the delta of the maximum luminance of 5 points. See Figure 4.
- All measurements are made with a Topcon BM-5A and SR-3 luminance meter.

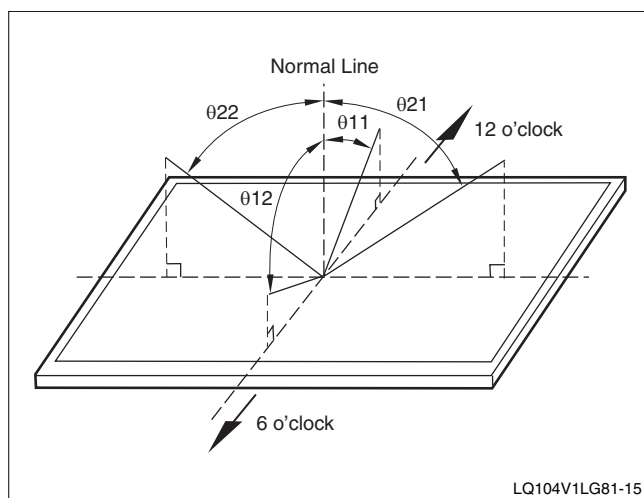


Figure 2. Viewing Angle

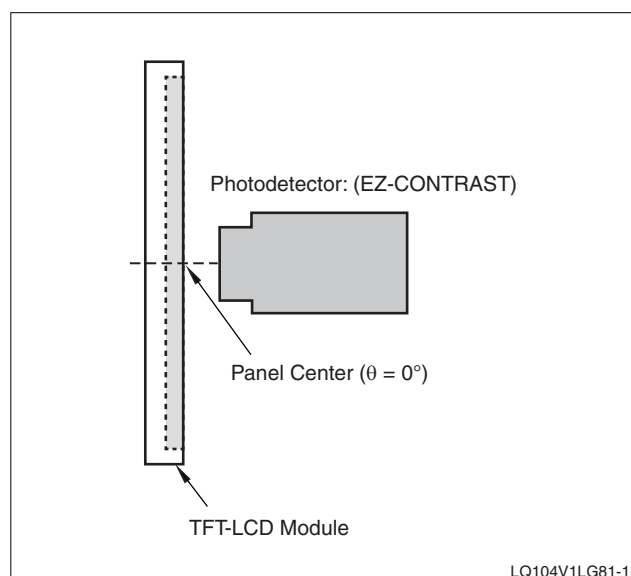


Figure 5. Viewing Angle Measurement Method

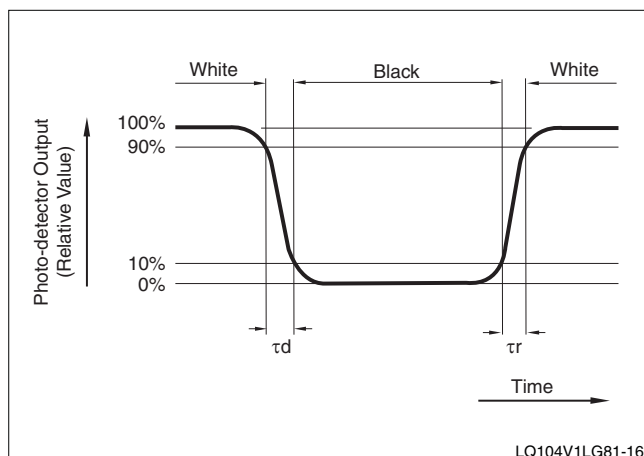


Figure 3. Response Time

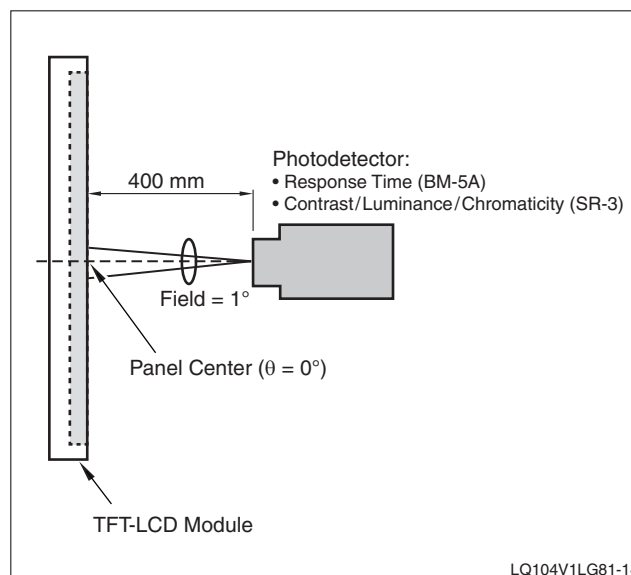


Figure 6. Contrast, Luminance, Response Time, and Chromaticity Measurement Method

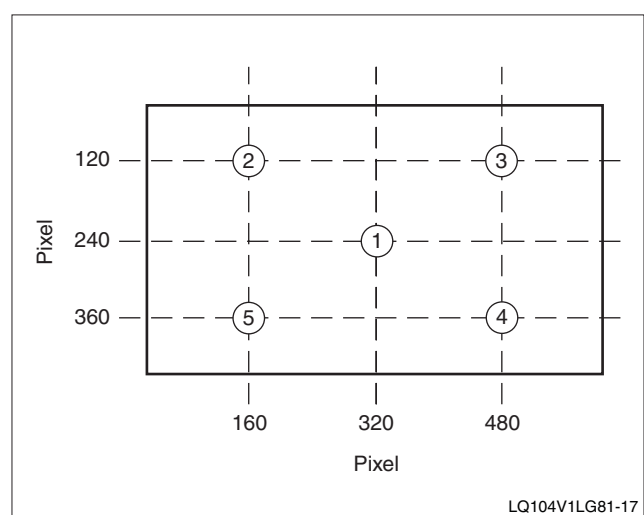


Figure 4. White Uniformity Measurement

ELECTRICAL SPECIFICATIONS - PANEL

Here are the Recommended Operating Conditions for this module.

$V_{CC} = +3.3\text{ V}$, $T_a = 25^\circ\text{C}$

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	1
Power Dissipation	I_{CC}		TBD	TBD	mA	2
Input Voltage Ripple	V_{RP}			(100)	mV P-P	$V_{CC} = 3.3\text{ V}$
Input Signal Voltage	V_{IH}	2.1		-	V	3
	V_{IL}			0.8	V	
Input Leakage Current	I_{OH}			(400)	μA	$V_{I2} = +3.3\text{ V}^3$
	I_{OL}	(-400)		-	μA	$V_{I2} = 0\text{ V}^3$
LVDS Reciever Input Voltage Range	V_L	0		2.4	V	
Differential Input Threshold Voltage	V_{TH}			$V_{CM} + 100$	mV	$V_{CM} = +1.2\text{ V}^4$
	V_{TL}	$V_{CM} - 100$		-	mV	

NOTES:

1. See *Power Supply Sequencing* for proper sequencing and maximum allowable V_{CC} dip conditions.
2. Power dissipation pattern is 64-gray bar pattern. See Figure 7. $V_{CC} = +3.3\text{ V}$, $f_{ck} = 25.175\text{ MHz}$, $T_a = 25^\circ\text{C}$
3. SCAN = LOW
4. V_{CM} = Common Mode Voltage. Applies to RXIN0-, RXIN0+, RXIN1-, RXIN1+, RXIN2-, RXIN2+, RXCLKIN-, RCLKIN+

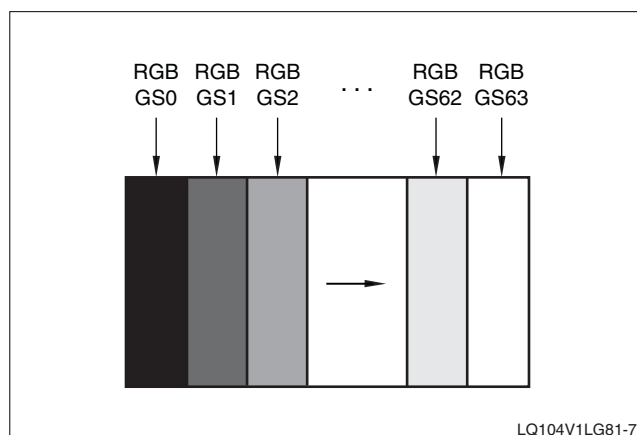


Figure 7. Power Dissipation Test Pattern

Power Supply Sequencing

This device requires proper supply sequencing on both startup and shutdown to prevent latching of the logic circuits. Refer to Figure 9.

PANEL POWER-UP

Panel Vcc must rise first. Sharp recommends holding Backlight Vdd LOW until the panel has initialized, to prevent unwanted patterns from being displayed.

- Vcc risetime from 10% to 90% must not take more than 10 ms nor less than 20 μ s. Data lines, XSTABY, VBR, and Backlight Vdd are held LOW during this time.
- Immediately after Vcc rises to nominal, but not more than 10 ms, send data to the panel.
- After 300 ms, apply Backlight Vdd.

PANEL POWER-DOWN

Sharp recommends switching Backlight Vdd off at least 200 ms before data to the panel ceases, to prevent unwanted patterns from being displayed.

- Immediately after data to the panel ceases, but not more than 1 second, Vcc falls.

CAUTION: Do not reapply Vcc within one second of power-down. Latchup can occur.

PANEL VCC DIP

Panel Vcc may not dip for more than 10 ms, and to a level no less than 2.5 V. If Vcc must dip longer than this and to a lower level, follow power-down sequencing.

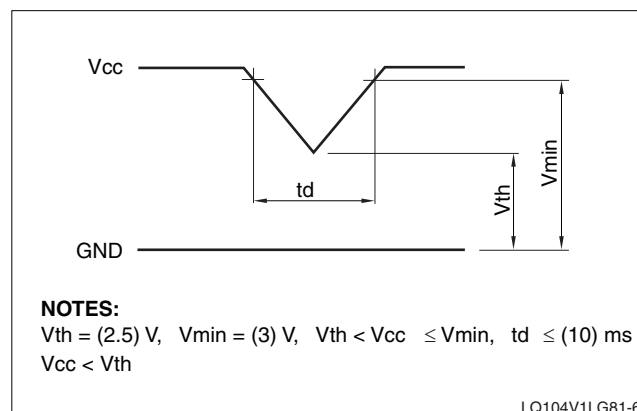


Figure 8. Power Supply Voltage Dip (MAX.)

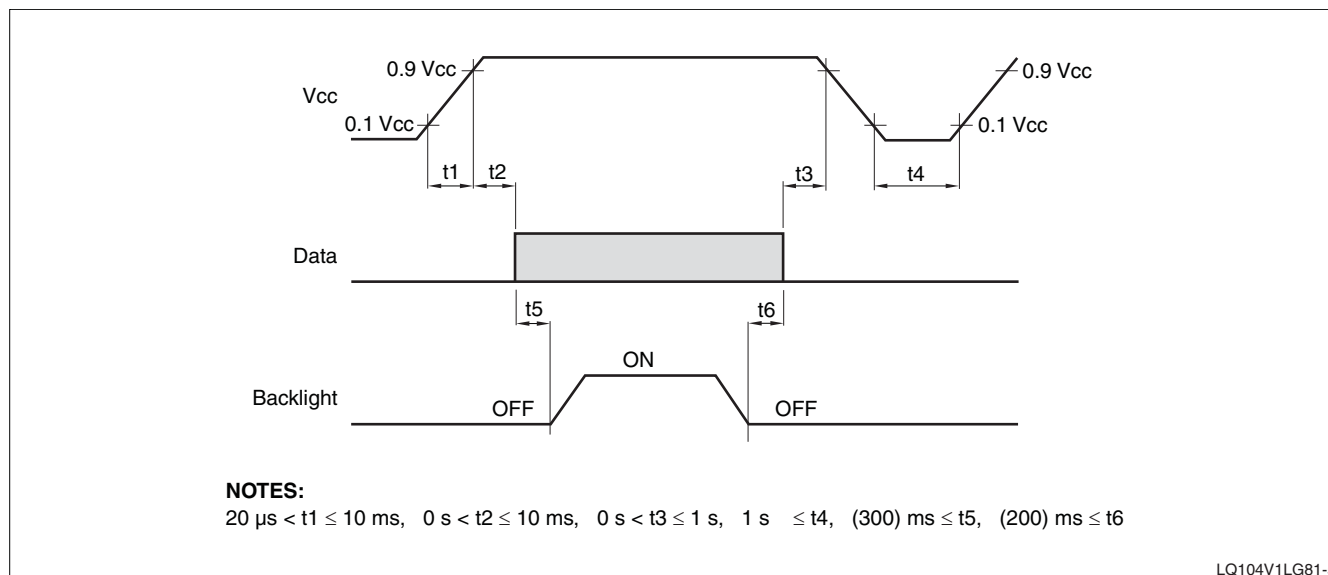


Figure 9. Panel Power Supply Sequencing

LED BACKLIGHT ELECTRICAL SPECIFICATIONS

Here are the Recommended Operating Conditions for the backlight in this module.

Vdd = +12 V, Ta = 25°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply Voltage	Vdd	10.2	12.0	13.8	V	1
Power Dissipation	IDD1		(450)	(650)	mA	2
	IDD2			10.0	μA	
Input Voltage Ripple	VRP, BL			(200.0)	mV P-P	Vdd = +12.0 V
XSTABY (HIGH)	VIH, BL1	9.0		Vdd	V	3
XSTABY (LOW)	VIL, BL1			0.4	V	3
VBR (HIGH)	VIH, BL2	9.0		Vdd	V	4
VBR (LOW)	VIL, BL2			0.4	V	4
PWM Frequency	fPWM	(200.0)		(1k)	Hz	4, 5
PWM Duty	DPWM	(10.0)		100.0	%	4, 5
Lifetime	L		(50,000)			6

NOTES:

1. See *Power Supply Sequencing*.
2. Power dissipation is measured at 100% duty. TYP. = Vdd = 12 V, MAX. = Vdd = 10.2 V.
3. XSTABY connected to 33 k Ω pull-down.
4. VBR connected to 33 k Ω pull-down.
5. See *PWM Drive*.
6. Point at which the luminance has fallen to 50% of initial value. This is a reference value for the backlight subassembly.

BACKLIGHT POWER-UP

Backlight Vdd rises first. Sharp recommends holding Backlight Vdd LOW until the panel has initialized, to prevent unwanted patterns from being displayed.

- Vdd risetime from 10% to 90% must not take more than 200 ms nor less than 20 μ s. XSTABY and VBR are held LOW during this time.
- Immediately (no maximum time) after Vdd rises to nominal, release XSTABY.
- After 10 ms (no maximum time), send data to the PWM.
- Backlight LED line may rise concurrently with data to the PWM, but there is no maximum time.

BACKLIGHT POWER-DOWN

- Backlight LED line may be switched off simultaneously with VBR, XSTABY and Backlight Vdd; however if there is any latency, XSTABY should fall last before Backlight Vdd falls.

CAUTION: Do not reapply Vdd within 200 ms of power-down. Latchup can occur.

PWM Drive

The backlight driver built into this panel has VBR as its input line, where duty cycle of a square wave controls display brightness. Brightness is directly related to the duty cycle (t_1/t_2), so 100% duty = full brightness and 0% duty = minimum brightness.

Recommended PWM dimming frequency (f_{PWM}) is 100 μ s or less. When the frequency is greater than this time, some degradation in display clarity may occur. See Figure 10.

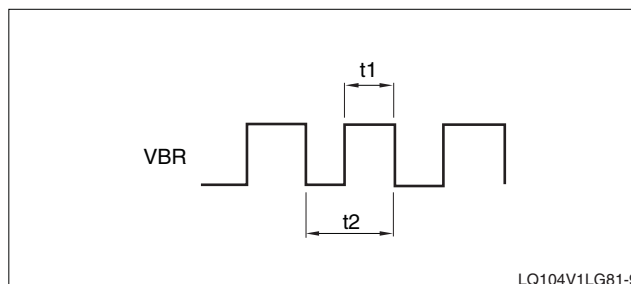


Figure 10. PWM Duty Cycle

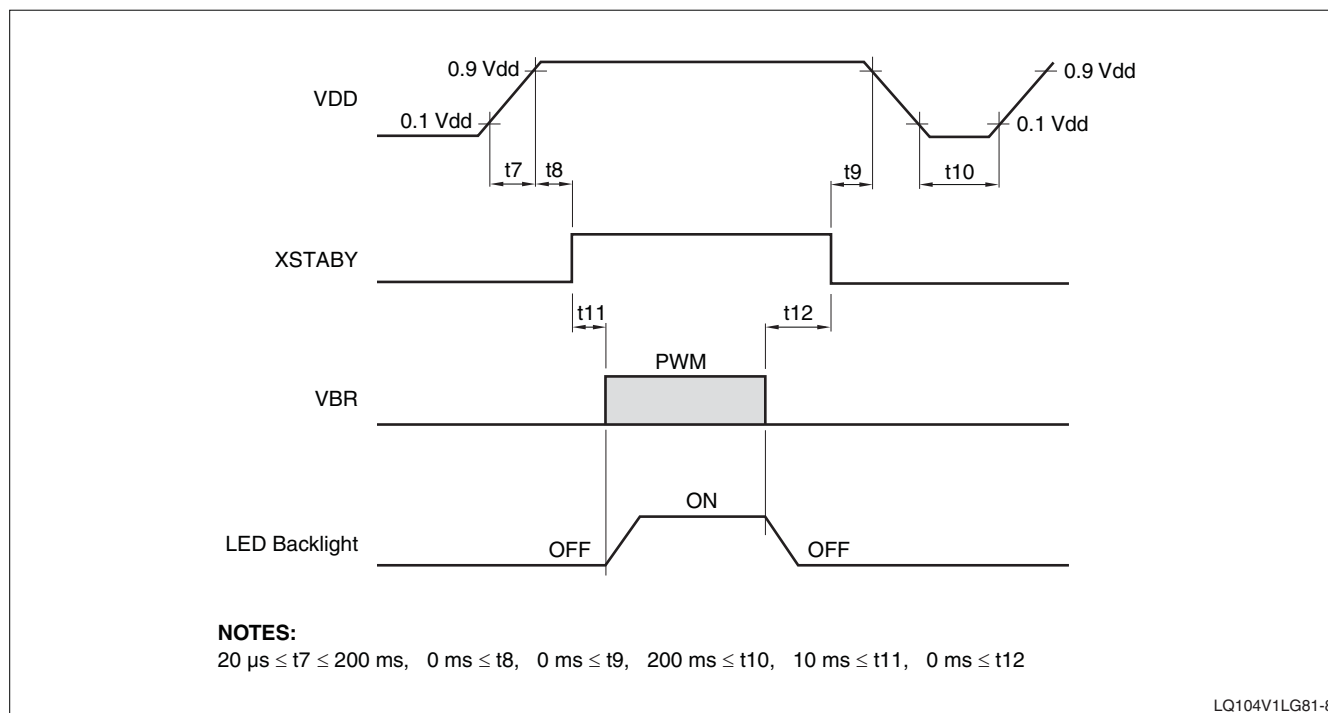


Figure 11. Backlight Power Sequencing

SIGNAL DESCRIPTIONS

Input signal characteristics are given in Table 3;
refer to Figure 12 for timing diagrams.

All measurements are at V_{dd} = 2.7 V to 3.6 V, V_{ddIO}
= 1.65 V to 3.6 V, GND = 0 V, T_a = 25°C.

Table 3. Signal Timing

SIGNAL	SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTES
Clock	1/Tc	Frequency	(23)	25.18	(28.33)	MHz	
Horizontal Sync Signal (Hsync)	TH	Cycle	(750)	800	(900)	clock	
			26.50	31.78	-	μs	
	THP	Pulse width	2	96	200	clock	
	THS	Data start position	(104)	(104)	(104)	clock	1
Vertical Sync Signal (Vsync)	TVH	Setup time	0	-	TH-THP	clock	
	TV	Cycle	(515)	525	(560)	line	
	1/TV	Frequency	(56)	60	(70)	Hz	2
	TVP	Pulse width	1	2	32	line	
	TVS	Data start position	(34)	(34)	(34)	line	
Enable Signal	TEP	Pulse width	640	640	640	clock	
	THE	Hsync-Enable signal phase difference	(44)	-	(TH-664)	clock	
Display Period	THD	Horizontal	640	640	640	clock	
	TVD	Vertical	480	480	480	line	

NOTES:

1. When ENAB is tied LOW, display start time is on Clock 104, as shown in Figure 13. Do not tie ENAB HIGH.
2. If Vsync frequency is too low, the display may exhibit flicker and lower quality.
3. Parens indicate reference values.

Timing Diagrams

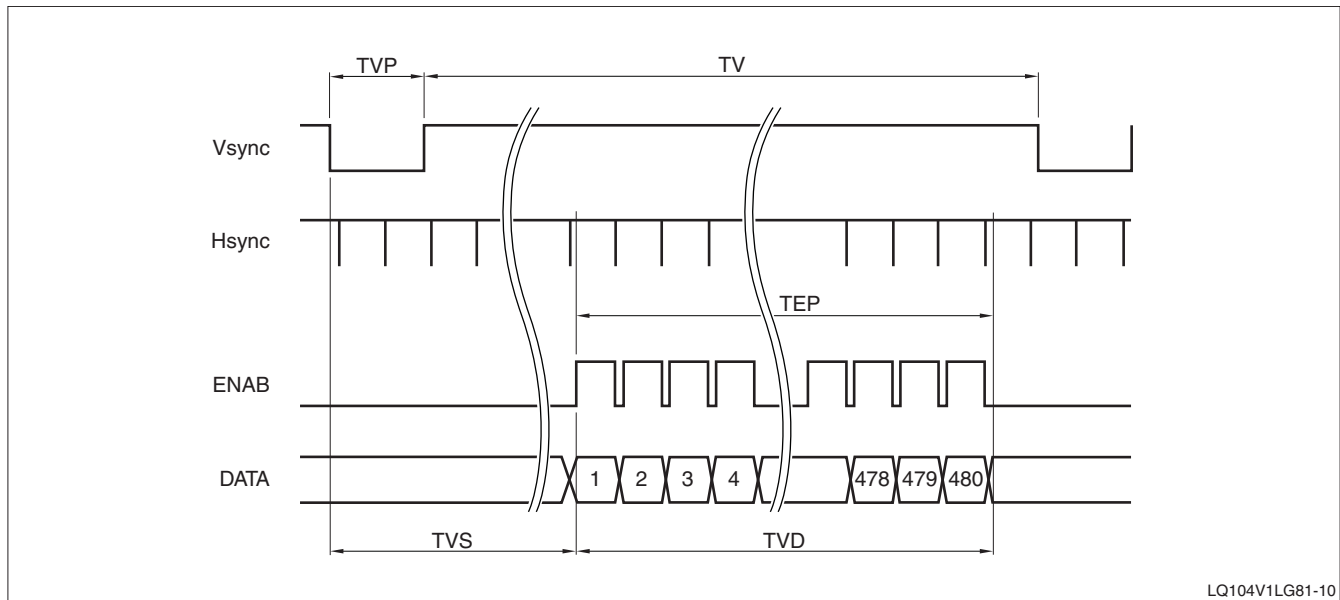


Figure 12. Signal Timing, Vertical Rate

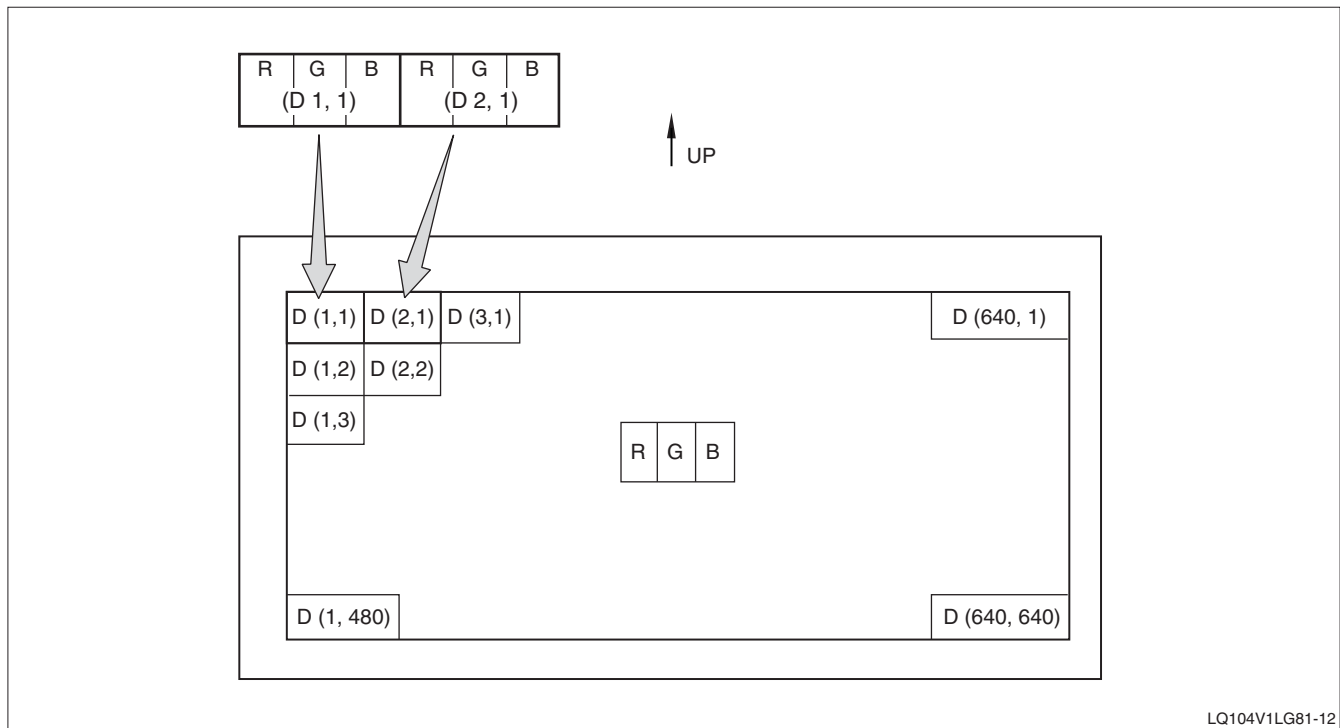


Figure 13. Signal Timing, Horizontal Rate

LVDS SYSTEM

The interface in this module allows the use of 8-bit or 6-bit signals.

8-bit Signals

Figure 14 is a block diagram of the 8-bit mode, and Table 4 gives bit mapping for THine Electronics THC63LVDM83R; a corresponding transmitter.

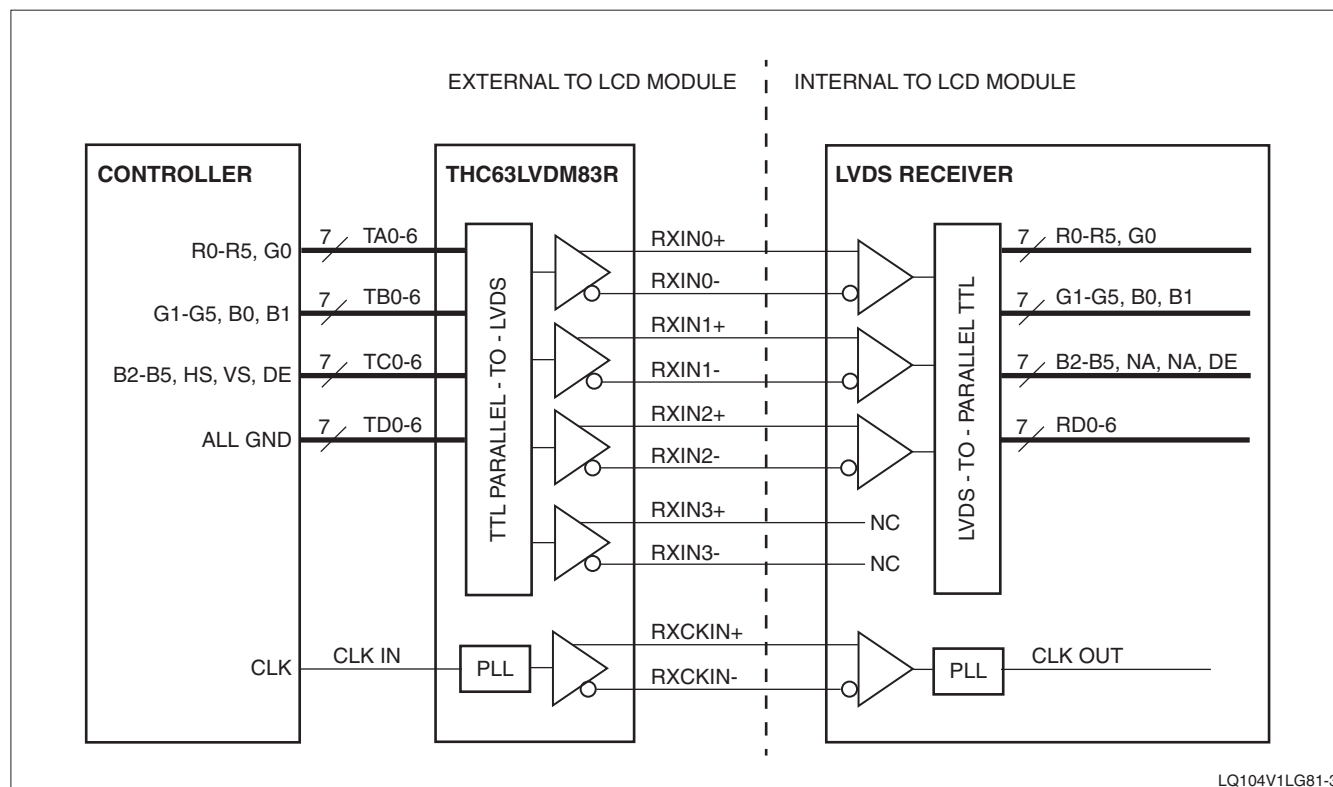


Figure 14. 8-bit Mode Block Diagram

Table 4. 8-bit Transmitter Map

TRANSMITTER		FUNCTION
PIN NO	DATA	
51	TA0	RO (LSB)
52	TA1	R1
54	TA2	R2
55	TA3	R3
56	TA4	R4
3	TA5	R5 (MSB)
4	TA6	GO (LSB)
6	TBO	G1
7	TB1	G2
11	TB2	G3
12	TB3	G4
14	TB4	G5(MSB)
15	TB5	BO(LSB)
19	TB6	B1

Table 4. 8-bit Transmitter Map (Continued)

TRANSMITTER		FUNCTION
PIN NO	DATA	
20	TC0	B2
22	TC1	B3
23	TC2	B4
24	TC3	B5(MSB)
27	TC4	HS
28	TC5	VS
30	TC6	DE
50	TDO	GND
2	TD1	GND
8	TD2	GND
10	TD3	GND
16	TD4	GND
18	TD5	GND
25	TD6	GND

6-bit Signals

Figure 15 is a block diagram of the 6-bit mode, and Table 5 gives bit mapping for THine Electronics THC63LVDM63A; a corresponding transmitter.

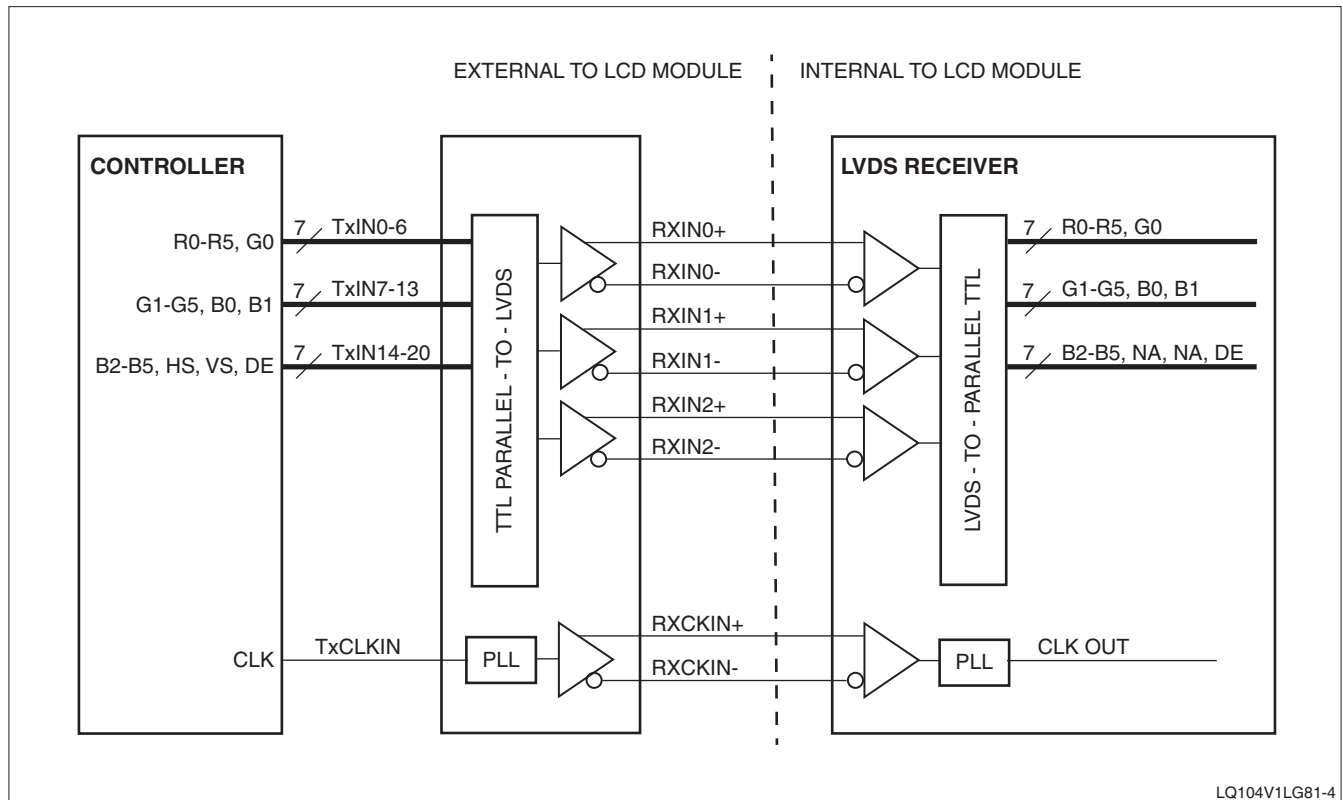


Figure 15. 6-bit Mode Block Diagram

Table 5. 6-bit Transmitter Map

TRANSMITTER		FUNCTION
PIN NO	DATA	
24	TxIN0	R0 (LSB)
26	TxIN1	R1
27	TxIN2	R2
29	TxIN3	R3
30	TxIN4	R4
31	TxIN5	R5 (MSB)
33	TxIN6	G0 (LSB)
34	TxIN7	G1
35	TxIN8	G2
37	TxIN9	G3
39	TxIN10	G4
40	TxIN11	G5 (MSB)
41	TxIN12	B0 (LSB)

Table 5. 6-bit Transmitter Map (Continued)

TRANSMITTER		FUNCTION
PIN NO	DATA	
43	TxIN13	B1
45	TxIN14	B2
46	TxIN15	B3
47	TxIN16	B4
1	TxIN17	B5 (MSB)
2	TxIN18	HS
4	TxIN19	VS
5	TxIN20	DE

Data Cycle

Figure 16 illustrates one data cycle. It starts at DE (Data Enable).

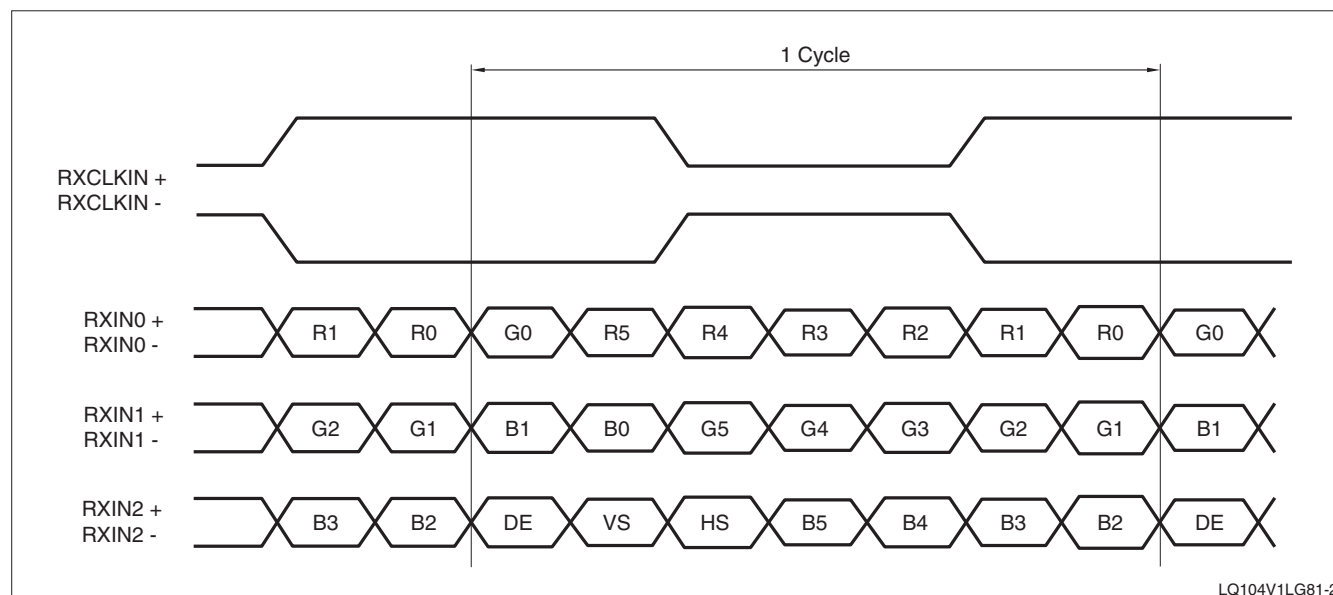


Figure 16. One Data Cycle

Input Signal and Color Matrix

Table 6 shows the signal and color matrix for this module. A 64-level gray scale is possible even with a 6-bit input. Total colors displayable are 262,144.

Table 6. Signal and Color Matrix

COLORS and GRAYSCALE		DATA SIGNAL																		
		GRAY-SCALE	R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	B4	B5
Basic Colors	Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	-	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Green	-	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	-	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Red	-	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	-	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	-	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red Grayscale	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	(Darker)	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
	(Brighter)	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green Grayscale	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	(Darker)	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
	(Brighter)	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
	⋮	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
	Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue Grayscale	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
	(Darker)	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
	(Brighter)	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
	⋮	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
	Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Physical Addressing

Figure 17 illustrates the physical address schema for this module.

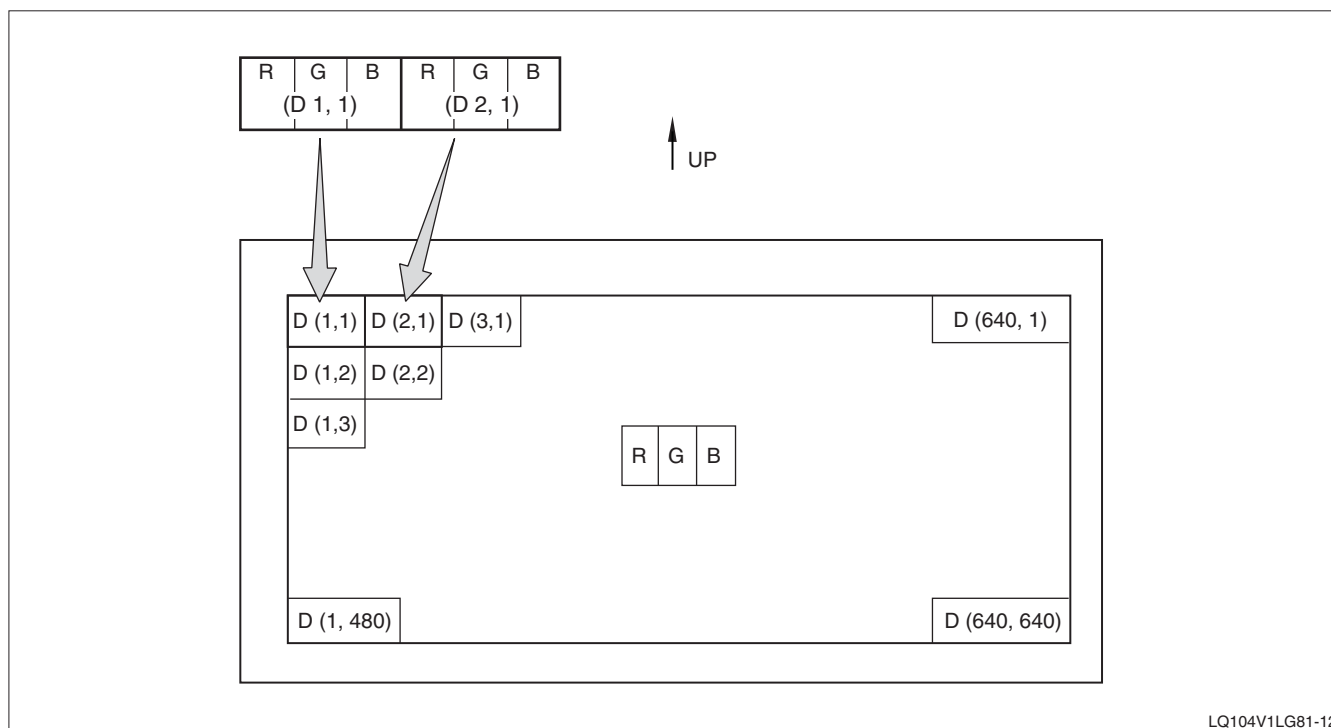


Figure 17. Display Data Addressing

DESIGN NOTES

1. This device is static sensitive. Handle it only in a static-safe environment. Always connect a ground for stability against EMI and external noise.
2. Do not press on the surface of the module, and do not stack modules in such a way that pressure will be applied to the surfaces or to the connector area. The safest place for temporary storage of modules is in their shipping tray.
3. The Specifications for this part and this Application Information document give definite environmental, electrical, and signal drive conditions for the operation and storage of this module. Operating it or storing it outside of these given limits can reduce image quality, shorten its life, or cause it to fail altogether.
4. When considering use of this module in an inverted position, note that the maximum viewing angle is in the 6 o'clock direction. Inverting the module may compromise grayscale performance.
5. When possible, avoid long-term, fixed-pattern displays to prevent stuck pixels.
6. When considering an enclosure for this module, do not allow stress to be applied to the circuit board on the back of this module; likewise constant pressure on the back of the module may result in erratic or otherwise unacceptable display performance.
7. Support for the module should be designed to avoid stress exceeding the maximums given in the Specifications. Do not allow the mounting design to apply warping or twisting forces to the module.
8. This module is not made to be disassembled. Doing so may cause permanent damage. Do not remove any black tape on the module.
9. When installing a protective covering over the module, do not allow it to apply pressure to the optical interface areas on the fringe of the module; doing so can degrade display quality.
10. The front polarizer and the module itself can be affected by outgassing of oxidation and deoxidation gasses, epoxy resin amine system curing agents, production handling materials, silicon adhesives (dealcoholization and oxime systems) tray cleaning agents (azo-compounds). Sharp recommends confirming performance with your materials and systems.
11. The module can be affected by reagents, solvents, adhesives, and resins; all can cause corrosion and discoloration of the modules. Sharp does not recommend using the module in such an environment.
12. The liquid crystal material in these modules will deteriorate from UV radiation. Do not store or operate the modules in direct sun or under strong UV radiation without some form of protection.
13. This part is shipped with all adjustments optimized and in compliance with Specifications. Do not change any adjustments on the module, as doing so will cause the module to not perform to published Specifications.

HANDLING AND STORAGE

1. Handle modules with care as glass is used in the modules. Impacts to corners and sides should be avoided as they can cause cracks or chips.
2. The liquid crystal material in this module is injurious to humans. Do not allow it to get into the eyes or mouth. If any liquid crystal material gets on skin or clothing, immediately wash it out with soap and water.
3. The polarizer film on the front surface of this module is susceptible to damage from scratches or by allowing water to stand on the surface of the module. Any water on the surface must be immediately removed as it can cause defects or color changes if allowed to remain for long periods.
4. To clean the glass surface of the module, wipe it with absorbent cotton or a soft cloth. If further cleaning is necessary, use isopropyl alcohol and wipe lightly on the surface of the module only.
5. This module is RoHS compliant, and does not use any ODS (1,1,1-Trichloroethane, CCL4) in its materials or in its production processes.
6. When discarding this module, dispose of it as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal cell contains an extremely small amount of liquid crystal (approx.100 mg) and therefore will not leak; even if the panel should break.

Storage

1. Store these devices at a temperature range between 0°C and 40°C, at 95% RH or less.
2. Do not allow more than 10 days of this storage to be at 40°C, at 95% RH.
3. Use within 1 year.
4. Store pallets of this product with moderate ventilation around all sides. Do not place cartons directly on a floor or against a wall.
5. The liquid crystal material in this module will solidify if stored below the rated temperature, and will become an isotropic liquid if stored above the rated storage temperatures. After such storage, the material may not return to its original properties.
6. When storing this module, keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light. Recommended storage is in a dark place.

PACKING AND LABELING

Each module will carry a module serial number label (see Figure 18) and a backlight serial number label (see Figure 20). Lot number determination is as shown in Figure 19.

RELIABILITY

Normal operating conditions: Temperature: 15°C to 35°C, Humidity: 45% to 75%, Atmospheric pressure: 86 to 106 kpa.

Pass: No change to display function.

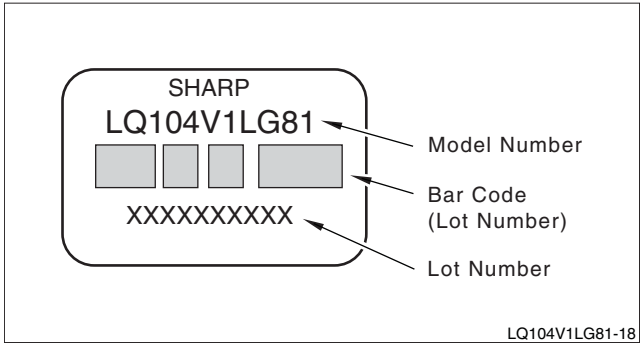


Figure 18. Panel Serial Number Sticker

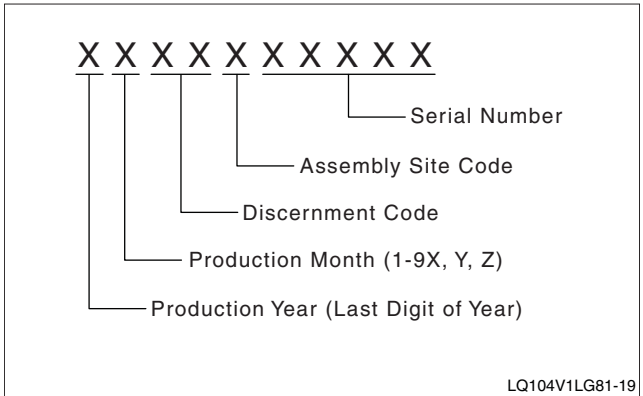


Figure 19. Lot Number Breakdown

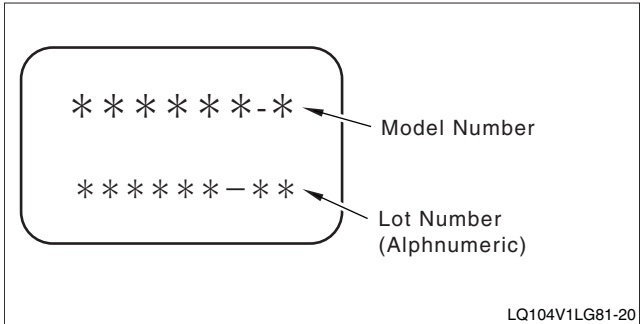


Figure 20. Backlight Serial Number Sticker

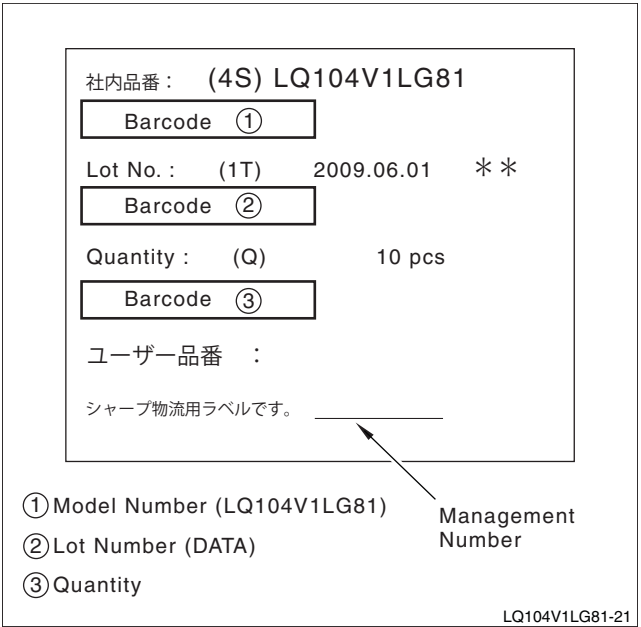


Figure 21. Box Label Sticker

Table 7. Reliabiltiy Tests

NO.	TEST	CONDITIONS
1	High Temperature Storage	Ambient temperature 80°C, 240 h
2	Low Temperature Storage	Ambient temperature -30°C, 240 h
3	High Temperature + High Humidity Operation	Ambient temperature 40°C, Humidity 95% 240 h (Non condensing)
4	High Temperature Operation	Panel surface (Active Area) 80°C 240H
5	Low Temperature Operation	Ambient temperature -30°C 240H
6	Vibration	Sine wave frequency: 10 to 57 Hz Vibration width (one side): 0.076 mm 57 to 500 Hz, Gravity: 9.8m/s² Sweep time: 11 minutes Test period: X, Y, Z direction, 1 h; total 3 h
7	Shock	Max. gravity: 490 m/s ² Pulse width: 11 ms Direction: ±X, ±Y, ±Z Test period: once in each direction

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

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**NORTH AMERICA**

SHARP Microelectronics of the Americas
5700 NW Pacific Rim Blvd.
Camas, WA 98607, U.S.A.
Phone: (1) 360-834-2500
Fax: (1) 360-834-8903
www.sharpsma.com

EUROPE

SHARP Microelectronics Europe
Division of Sharp Electronics (Europe) GmbH
Sonninstrasse 3
20097 Hamburg, Germany
Phone: (49) 40-2376-2286
Fax: (49) 40-2376-2232
www.sharpsme.com

JAPAN

SHARP Corporation
Electronic Components & Devices
22-22 Nagaike-cho, Abeno-Ku
Osaka 545-8522, Japan
Phone: (81) 6-6621-1221
Fax: (81) 6117-725300/6117-725301
www.sharp-world.com

TAIWAN

SHARP Electronic Components
(Taiwan) Corporation
8F-A, No. 16, Sec. 4, Nanking E. Rd.
Taipei, Taiwan, Republic of China
Phone: (886) 2-2577-7341
Fax: (886) 2-2577-7326/2-2577-7328

SINGAPORE

SHARP Electronics (Singapore) PTE., Ltd.
438A, Alexandra Road, #05-01/02
Alexandra Technopark,
Singapore 119967
Phone: (65) 271-3566
Fax: (65) 271-3855

KOREA

SHARP Electronic Components
(Korea) Corporation
RM 501 Geosung B/D, 541
Dohwa-dong, Mapo-ku
Seoul 121-701, Korea
Phone: (82) 2-711-5813 ~ 8
Fax: (82) 2-711-5819

CHINA

SHARP Microelectronics of China
(Shanghai) Co., Ltd.
28 Xin Jin Qiao Road King Tower 16F
Pudong Shanghai, 201206 P.R. China
Phone: (86) 21-5854-7710/21-5834-6056
Fax: (86) 21-5854-4340/21-5834-6057
Head Office:
No. 360, Bashen Road,
Xin Development Bldg. 22
Waigaoqiao Free Trade Zone Shanghai
200131 P.R. China
Email: smc@china.global.sharp.co.jp

HONG KONG

SHARP-ROXY (Hong Kong) Ltd.
3rd Business Division,
17/F, Admiralty Centre, Tower 1
18 Harcourt Road, Hong Kong
Phone: (852) 28229311
Fax: (852) 28660779
www.sharp.com.hk
Shenzhen Representative Office:
Room 13B1, Tower C,
Electronics Science & Technology Building
Shen Nan Zhong Road
Shenzhen, P.R. China
Phone: (86) 755-3273731
Fax: (86) 755-3273735