1 General Description

The AS5130 is a contactless magnetic rotary encoder for accurate angular measurement over a full turn of 360°. It is a system-on-chip, combining integrated Hall elements, analog front end and digital signal processing in a single device. To measure the angle, only a simple two-pole magnet, rotating over the center of the chip, is required. The magnet may be placed above or below the IC. The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8 bit = 256 positions per revolution. This digital data is available as a serial bit stream and as a PWM signal. The AS5130 can be operated in pulsed mode (Vsupply=off), which reduces the average power consumption significantly. During Vsupply=off, the measured angle can be stored using an internal storage register supplied by a low power voltage line. . This mode achieves very low power consumption during polling of the rotary position of the magnet. The motion detection feature wakes up an external system, if the magnet's position changes. The device is capable of counting the amount of magnet revolutions. The multi turn counter value is stored in a register and can be read in addition to the angle information. Furthermore any arbitrary position can be set as zero-position. The system is tolerant to misalignment, air gap variations, temperature variations and external magnetic fields and high reliability due to non-contact sensing.

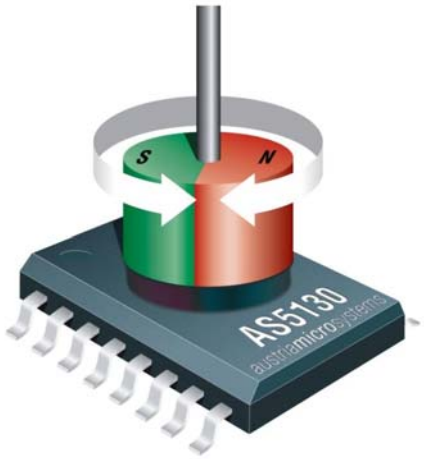


Figure 1: Typical arrangement of AS5130 and magnet

1.1. Applications

- Ignition key position sensing
- Steering wheel position sensing
- Transmission gearbox encoder
- Front panel rotary switches
- Replacement of potentiometers

1.2. Key Features

- 360°contactless angular position encoding
- Two digital 8-bit absolute outputs:
  - Serial interface and
  - Pulse width modulated (PWM) output
- User programmable zero position
- High speed: up to 30000 rpm
- Failure detection mode for magnet placement monitoring and loss of power supply
- Wide temperature range: - 40°C to + 125°C
- Multi Turn counter / Movement detection
- Small Pb-free package: SSOP-16 (5,3mm x 6,2mm)
- Automotive qualified to AEC-Q100, grade 1

1.3. Benefits

- Complete system-on-chip
- Flexible system solution providing absolute angle position, with serial data and PWM output,
- Ideal for applications in harsh environments due to magnetic
- sensing principle,
- High reliability due to non-contact sensing,
- Robust system, tolerant to misalignment, airgap variations, temperature variations and external magnetic fields

1.4. Block Diagram

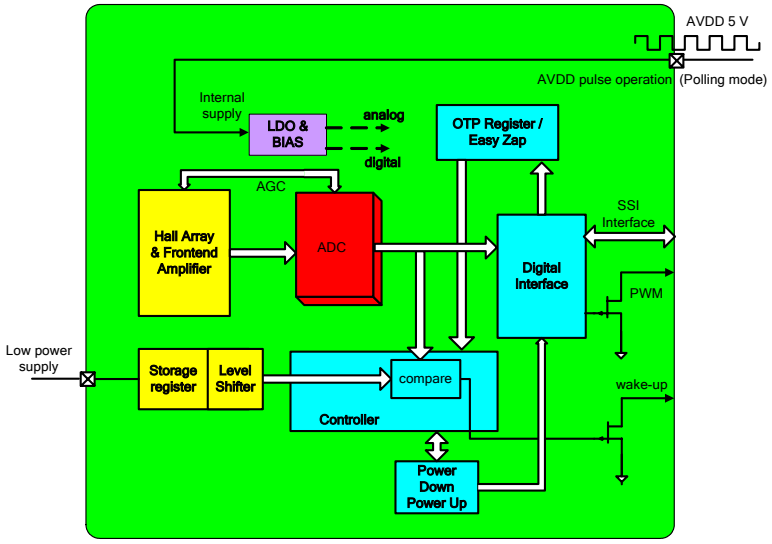


Figure 2: AS5130 Block diagram

5 Package and Pinout

The AS5130 is available in SSOP16 5.3mm.

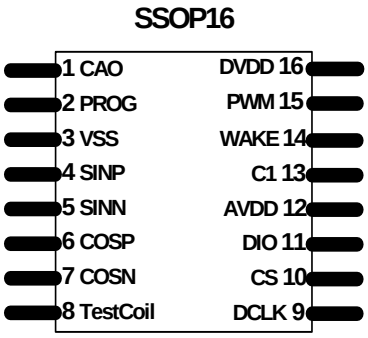


Figure 3: AS5130 Pin out

Pin	Pin Name	Pin Type	Notes / Library Cell Name
1	CAO	DO_T	Indicates, if the magnetic field is present. If the field is too low, the signal is HI.
2	PROG	S	OTP Programming Pad, programming voltage. For normal operation it must be left unconnected.
3	VSS	S	Supply Ground.
4	SINP	AIO	Used for factory testing. For normal operation it must be left unconnected.
5	SINN	AIO	Used for factory testing. For normal operation it must be left unconnected.
6	COSP	AIO	Used for factory testing. For normal operation it must be left unconnected.
7	COSN	AIO	Used for factory testing. For normal operation it must be left unconnected.
8	Test Coil	AIO	Test pin. Must be left unconnected.
9	DCLK	DI_ST	Clock source for SSI communication. Schmitt trigger input.
10	CS	DI_ST	Chip select for SSI, active high. Schmitt trigger input.
11	DIO	DIO	Data input / output for SSI communication.
12	AVDD	S	Positive Supply Voltage 5V.
13	C1	DIO	Test mode selector. For normal operation it must be connected to VSS.
14	WAKE	AO	Interrupt output, used for polling mode. Open Drain NMOS. Use pull-up resistor with >1.5kOhm.
15	PWM	DO	Pulse Width Modulation output. 0.5us width step per LSB.
16	DVDD	AIO	Pin to connect to low power supply for polling mode. Must be connected to VSS in normal mode.

PIN Types:

S	supply pad	DO	digital output
AO	analog output	DI_ST	digital input with Schmitt trigger
AIO	analog input / output	DO_T	digital output with tri-state
DIO	digital input/output		

6 Parameter and Feature List

PARAMETER	DESCRIPITION
Supply Voltage:	5V +/- 10%
Supply Current	Normal operating mode: I <19mA. Power consumption is inversely proportional to the magnetic field strength provided. The minimum supply current is 11mA.
Absolute Output; Serial Interface (SSI)	21-bit Synchronous Serial Interface, 5 command bits, 1 bit data information Lock, indicates whether or not ADC Data is valid, 6 data bits for AGC information, 8 data bits for angle, 1 Parity Even bit, indicates validation status of serial transmission data stream. See figure 8 for more details.
SSI Clock rate	≤ 6 MHz
Low power mode	Activated by SSI command. Device is non-operational, internal oscillator and voltage references are active. Operating current in low power mode: 2 mA. Fast wake up is possible from this state (<150µs).
Resolution and Accuracy	Resolution = 8 bit (1.406°) Accuracy ≤ ±2° with centered magnet. (1)
Transition Noise	< 1.4° peak-to-peak
PWM output	PWM will be permanently low when magnetic field is out of input range or the lock bit is set to low.
Digital Output Current	4mA @ VDD=5V
OTP register	46-bit OTP programming register. For programming of zero position and sensitivity / magnetic input range. Chip ID for exact backtracking.
ESD protection	± 2kV HBM
Movement Detection	Compares stored angular value (reference) with current measured value. If the difference between these values is larger than a threshold (e.g. 4LSB), an interrupt request will be set via the wake up pin.
Automotive qualification	AEC-Q 100

(1) Only valid at the gain settings 1.05 to 2.2. For 0.9 and 2.55 the accuracy is reduced.

7 General Device Specifications

7.1 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Positive Supply Voltage	AVDD	4.5	5.5	V	Except OTP programming
Polling Mode Supply Voltage	DVDD	3.6	5.5	V	(1)
Power Supply Current	IDD		19	mA	outputs unloaded
Ambient Temperature	T_{amb}	-40	125	°C	
Junction Temperature	T_J		150	°C	

7.2. Absolute Maximum Ratings (non Operating)

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage	AVDD	0.3	7	V	
Input Pin Voltage	VIN	VSS-0.5	AVDD	V	
Input Current (latchup immunity)	I_{scr}	-100	100	mA	Norm: Jedec 17
Electrostatic Discharge	ESD		+/-2	kV	Norm: MIL 883 E method 3015
Package Thermal Resistance SSOP-16	Θ_{JAS}		137.1	K/W	Still Air / Single Layer PCB
Package Thermal Resistance SSOP-16	Θ_{JAM}	70	86	K/W	Still Air / Multi Layer PCB, JEDEC Standard Testboard
Storage Temperature	T_{strg}	-55	125	°C	
Package body temperature	T_{body}		260	°C	Norm: IPC/JEDEC J-STD-020C, (2)(3)
Soldering conditions	T_{lead}				Norm: IEC 61760-1, soldering conditions
Humidity non-condensing		5	85	%	

(1) Only relevant for polling operation mode, supply voltage with capacitor of the integrated storage register during t_{off} phase of AVDD

(2) The reflow peak soldering temperature(body temperature) is specified according IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”

(3) The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn)

7.3. Magnet + AS5130

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Rotational Speed	n	-30000	30000	rpm	(4)
Resolution	N		8	bit	
Magnetic Input Range	B_i	32	75	mT	(1)
Magnetic Sensitivity of AGC	S	0.5	5	LSB/mT	AGC value available at SSI
Magnetic Offset	B_{DC}		4	mT	Magnetic stray field without gradient.
Power up time	T_{PwrUp}		2000	us	Startup from zero
			250		Startup with preset AGC (2)
			150		Startup from sleep power mode
Wake up output	$V_{out\_wake\ up}$		5	V	open drain output with tri-state behavior, see Fig. 10
Angle difference threshold for wake up generation.	$Wake_{LSB}$	0	127	LSB	(3)
Power down current @ Low Power Mode	IDD_{MLP}		2	mA	To be activated by SSI command 17 (go2sleep).
Propagation Delay	T_{Prop}		10	µs	Time between angle changing of magnet and output signal at SSI (when AGC is locked)

(1) Valid for use of full range of sensitivity. For customer trimming refer to 1.8.

(2) If supplied during t_{off} phase of AVDD from the external buffer capacitor via DVDD pin.

(3) Factory setting is 4 LSB, value is accessible by SSI in buffered register and can be changed by customer

(4) Frequencies above 1000 rpm causes an additional not specified DNL Error

7.4. Magnetic input range

The magnetic input range is defined by the AGC loop. This regulating loop keeps the Hall sensor output in the optimum range for low SNR by adjusting the Hall bias current. This loop can adjust to a magnetic field strenght variation of ±38%. The AGC output voltage is an indicator for the magnetic field.

The nominal magnetic field for a balanced AGC is defined by the Hall bias and the Hall sensitivity and can be set by a variable gain in the signal path. The gain can be set in 8 steps in the OTP or by the SSI in a mirror register. The resulting magnetic input range is a value of $B_{nominal}$±38% inside of a range of 32mT ... 75mT if the trimming is performed by the customer.

Setting	0	1	2	3	4	5	6	7
Binary	000	001	010	011	100	101	110	111
Gain A	0.9	1.05	1.2	1.4	1.65	1.9	2.2	2.55
B_{limit}	Max. 75mT							Min. 32mT

7.5. DC/AC Characteristics for Digital Inputs and Outputs

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
CMOS Input					
High level Input voltage	V_{IH}	0.7*VDD		V	
Low level Input Voltage	V_{IL}		0.3*VDD	V	
Input Leakage Current	I_{LEAK}		1	uA	
CMOS Output					
High level Output voltage	V_{OH}	VDD - 0.5		V	4 mA
Low level Output Voltage	V_{OL}		VSS + 0.4	V	4 mA
Capacitive Load	C_L		35	pF	
Slew Rate	t_{slew}		30	ns	(1)
Time Rise Fall	t_{delay}		15	ns	(1)

(1) condition external capacitive load C_L=35pF

external series resistance R= 0 Ohm

junction temperature T_J = 136 °C

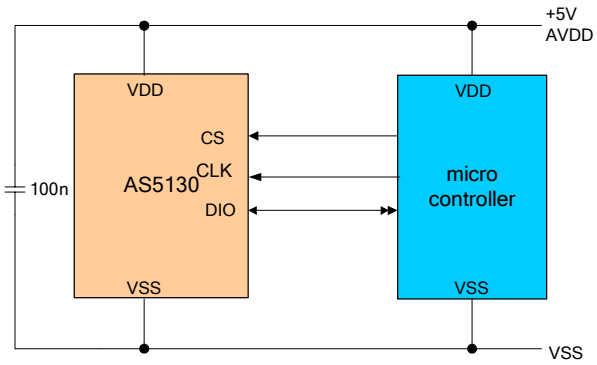
rise time of the internal driver t_rise = 3ns

fall time of the internal driver t_fall = 3ns

8 Connecting the AS5130

The AS5130 can be connected to an external controller in several ways:

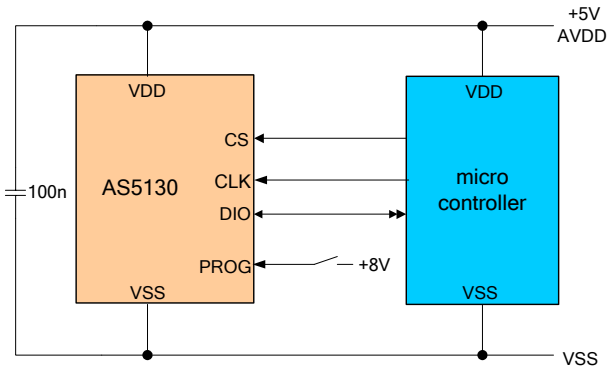
8.1. Serial 3-wire connection (default setting)



In this mode, the AS5130 is connected to the external controller via three SSI signals: Chip Select (CS), and Clock (CLK) input and DIO (Data) in/output. In this configuration it is possible to read and write data and to define different operation modes. The data transfer in all cases is done via the DIO port.

Figure 4: Standard SSI serial data transmission

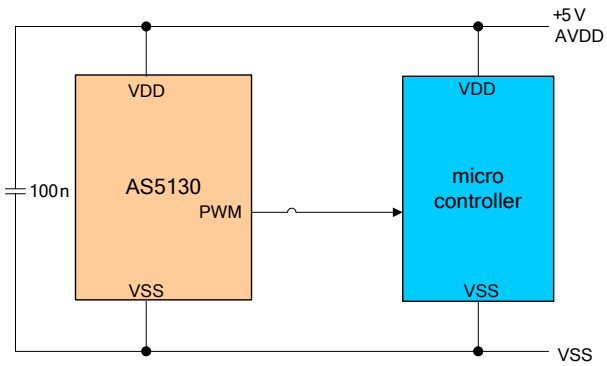
8.2. Serial 3-wire connection (OTP programming option)



As an option, the serial interface can be configured for programming the OTP register. A clock input (CLK) and DIO (Data) in/output as well as CS Pin will be required. In that mode, it is possible to write and read out data from the OTP Register. The data transfer is done via the DIO channel.
For programming the PROG pin must be connected to +8V. Analogue readout for trimming verification is mandatory.

Figure 5: Serial data transmission in continuous readout mode

8.3. 1-wire PWM connection



If the line (PWM) is used as angle output, the total number of connections can be reduced to three, including the supply lines. This type of configuration is especially useful for remote sensors. Low power mode is not possible in this configuration. If the AS5130 angular data is invalid, the PWM output will remain at low state.

Figure 6: Data transmission with pulse width modulated (PWM) output

8.4. Analog output

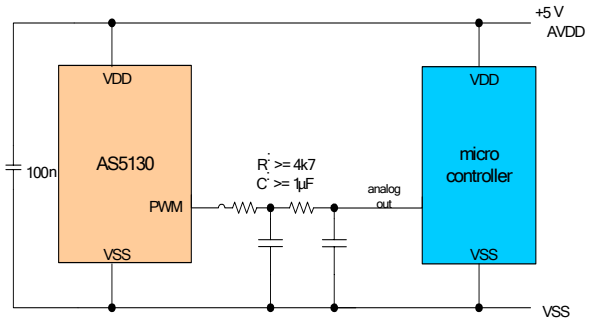


Figure 7: Ratiometric analog output

The AS5130 can generate a ratiometric analog output voltage by low-pass filtering the PWM output. Figure 7 shows a simple passive 2nd order low pass filter as an example. In order to minimize the ripple on the analog output, the cut-off frequency of the low pass filter should be well below the PWM base frequency.

9 Serial Synchronous Interface (SSI)

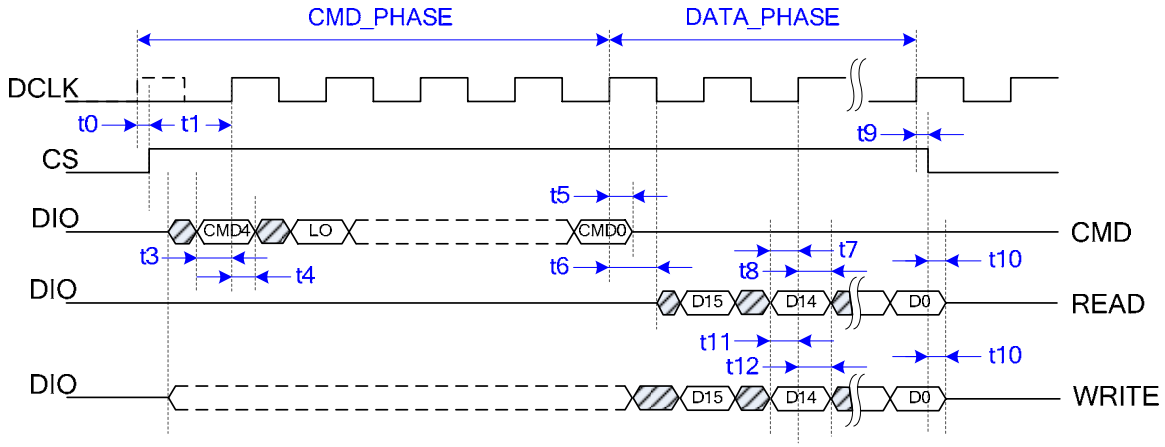


Fig. 8: Normal operation mode

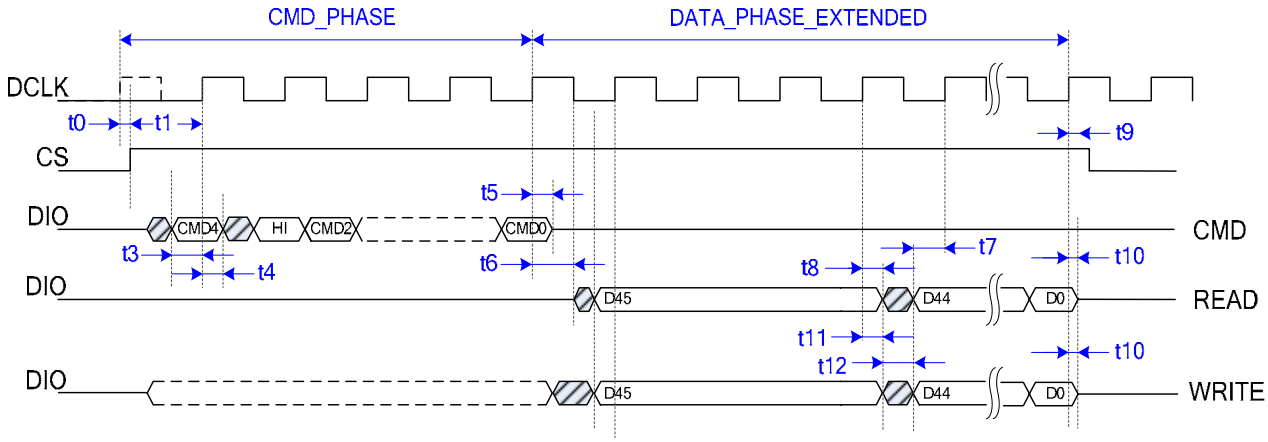


Fig. 9: Extended operation mode (for access of OTP only)

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
rising DCLK to CS	t0	15		ns	
chip select to positive edge of DCLK	t1	15		ns	
setup time data valid to positive edge of DCLK	t3	30		ns	
hold time data valid after positive edge of DCLK	t4	30		ns	
float time positive edge of DCLK for last command bit to bus float	t5	30	DCLK/2	ns	
bus driving time positive edge of DCLK for last command bit to bus drive	t6	DCLK/2	DCLK/2+30	ns	
setup time data bit data valid to positive edge of DCLK	t7	DCLK/2	DCLK/2+30	ns	
hold time data bit data valid after positive edge of DCLK	t8	DCLK/2	DCLK/2+30	ns	
hold time chip select positive edge DCLK to negative edge of chip select	t9	30		ns	
bus floating time negative edge of chip select to float bus	t10	0	30	ns	
setup time data bit @ write access data valid to positive edge of DCLK	t11	30		ns	
hold time data bit @ write access data valid after positive edge of DCLK	t12	30	DCLK/2+30	ns	

9.1. Commands of the SSI in Normal Mode

#	cmd	bin	mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23	WRITE CUST	10111	write	wlsb_6	wlsb_5	wlsb_4	wlsb_3	wlsb_2	wlsb_1	wlsb_0	gain_2	gain_1	gain_0	nc	nc	nc	nc	nc	nc
22	WD2COS	10110	write	xen_7	inv_7	xen_6	inv_6	xen_5	inv_5	xen_4	inv_4	xen_3	inv_3	xen_2	inv_2	xen_1	inv_1	xen_0	inv_0
21	SET TEST CFG 1	10101	write						gen_rst										
20	reserved	10100	write																
19	HYST_RST	10011	write	rst_otp			rst_multi			setHyst									
18	WD2SIN	10010	write	xen_7	inv_7	xen_6	inv_6	xen_5	inv_5	xen_4	inv_4	xen_3	inv_3	xen_2	inv_2	xen_1	inv_1	xen_0	inv_0
17	WRITE CONFIG	10001	write	go2sleep															
16	-	10000	write																
7	READ CUST	00111	read	wlsb_6	wlsb_5	wlsb_4	wlsb_3	wlsb_2	wlsb_1	wlsb_0	gain_2	gain_1	gain_0	nc	nc	nc	nc	nc	parity
6	RD2COS	00110	read	xen_7	inv_7	xen_6	inv_6	xen_5	inv_5	xen_4	inv_4	xen_3	inv_3	xen_2	inv_2	xen_1	inv_1	xen_0	inv_0
5		00101	read																
4	RD_BOTH	00100	read	Multiturn<7:0>								angle<7:0>							
3	STORE REF	00011	read	store_ok	vdd_ok	reg_set	nc	nc	nc	nc	angle_stored <7:0>								parity
2	RD2SIN	00010	read	xen_7	inv_7	xen_6	inv_6	xen_5	inv_5	xen_4	inv_4	xen_3	inv_3	xen_2	inv_2	xen_1	inv_1	xen_0	inv_0
1	RD_MULTI	00001	read	lock	agc <5:0>						multiturn <7:0>								parity
0	RD_ANGLE	00000	read	lock	agc <5:0>						angle <7:0>								parity

WD2COS / WD2SIN: xen_X disables Hall element X from the sensor array in the cosine or sine channel; xinv_X inverts the voltage output of Hall element X in the channels

RD2COS / RD2SIN: The Hall array configuration for cosine and sine channel can be read out by these commands, initial values are0.

SET TEST CFG 1: gen_rst HI triggers a digital reset.

WRITE CONFIG: go2sleep HI activates the sleep mode of the AS5130. The power consumption is significantly reduced. go2sleep LO returns to normal operation mode. During sleep mode, the lock bit in command 0 and command 1 is LO. Refer also to Error! Reference source not found..

WRITE CUST: With “wlsb_x” the threshold level for generation of a WAKE pulse is set (only important in polling mode). The initial value is 4 LSB. No value lower than 4 LSB can be set. The maximum value is 127 LSB.
“gain_x” sets the gain in the signal path (see Error! Reference source not found.)

HYST_RST: “setHyst” enables an additional hysteresis of the digital output signal. It is enabled by default. Only after 2 consecutive equal signals the output is changed.
“rst_otp” forces the IC to read out the OTP in polling mode. This reset has to be performed after initial startup and every WAKE signal.
“rst_multi” resets the multi turn counter to 0.

READ CUST: With this command “wlsb_x” and “gain_x” can be read out.

RD_BOTH: Angle and multi turn counter value can be read out simultaneously by this command. Due to limited data size, the parity bit is not available in this command.

STORE REF: This command stores the actual angle as reference angle in the storage registers (only important in polling mode). The output is the stored angle (angle_stored), a flag, if the voltage at DVDD is OK (store_ok), a flag, if the supply voltage is OK (vdd_ok) and a check bit, if the register was written.

RD_MULTI: Command for read out of multi turn register (multiturn) and AGC value (agc). “Lock” indicates a locked ADC and “parity” an even parity checksum.

RD_ANGLE: Command for read out of angle value and AGC value (agc). “Lock” indicates a locked ADC and “parity” an even parity checksum.

9.2. Commands of the SSI in Extended Mode

For programming or readout of the OTP data, the chip has to be started with DVDD at a low voltage (polling mode off or cap discharged) or the OTP reset has to be performed. If not, the OTP is not read out and the OTP data not available.

#	cmd	bin	mode	<45:44>	<43:32>	<31:28>	<27:26>	<25>	<24:23>	<22:20>	<19:16>	<15:12>	<11:9>	<8>	<7:0>
31	WRITE_OTP	11111	xt write	OTP Test	ID			OTP lock	Vref	Hall Bias	Osc	Redundancy	Sensitivity	Wake enable	Zero Angle
30		11110	xt write												
29		11101	xt write												
28		11100	xt write												
27		11011	xt write												
26		11010	xt write												
25	PROG_OTP	11001	xt write	OTP Test	ID			OTP lock	Vref	Hall Bias	Osc	Redundancy	Sensitivity	Wake enable	Zero Angle
24		11000	xt write												
15	RD_OTP	01111	xt read	OTP Test	ID			OTP lock	Vref	Hall Bias	Osc	Redundancy	Sensitivity	Wake enable	Zero Angle
14		01110	xt read												
13		01101	xt read												
12		01100	xt read												
11		01011	xt read												
10		01010	xt read												
9	RD_OTP_ANA	01001	xt read												
8		01000	xt read												

WRITE OTP: Writing of the OTP register. The written data is volatile. “Zero Angle” is the angle, which is set for zero position. “Wake enable” enables the polling mode. “Sensitivity” is the gain setting in the signal path (see Error! Reference source not found.). “Redundancy is a number of bits, which allows the customer to overwrite one of the customer OTP bits <0:11>. Refer to Error! Reference source not found. for further information.

PROG_OTP: Programming of the OTP register. Only Bits <0:15> can be programmed by the customer.

RD_OTP: Read out the content of the OTP register. Data written by WRITE_OTP and PROG_OTP is read out.

RD_OTP_ANA: Analog read out mode. The analog value of every OTP bit is available at pin 2 (PROG), which allows for a verification of the fuse process. No data is available at the SSI.

9.2.1. OTP Programming

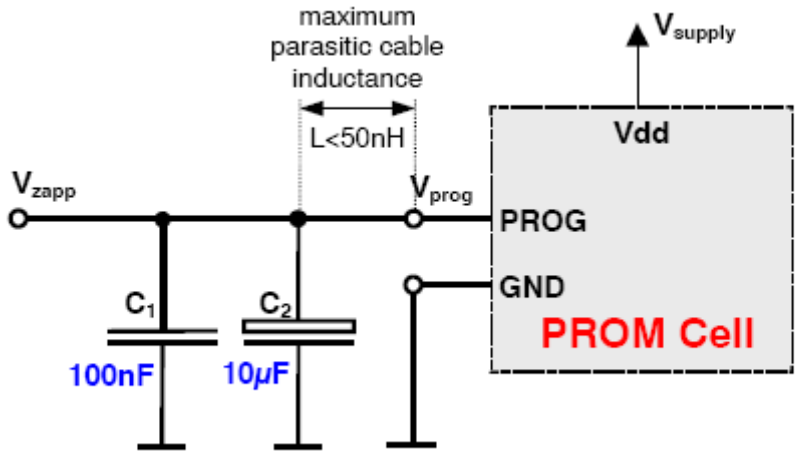


Fig. 10: external circuitry for OTP programming

For programming of the OTP, an additional voltage has to be applied to the pin PROG. It has to be buffered by a fast 100nF capacitor (ceramic) and a 10µF capacitor. The information to be programmed is set by command 25. The OTP bits 16 until 45 are used for AMS factory trimming and can not be overwritten.

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	VDD	5	5.5	V	
Ground level	GND	0	0	V	
Programming Voltage	V_zapp	8	8.5	V	At pin PROG
Temperature	T_zapp	0	85	°C	
CLK Frequency	f_clk		100	kHz	At pin DCLK

After programming an analog readout is mandatory. The capacitors and the programming voltage have to be removed from pin PROG and the voltage at PROG measured analogue. Command 9 will start the analogue readout and the programmed bits will be represented by voltage levels at PROG.

Parameter	Description	Min	Max	Unit
Logic 1	Voltage at PROG representing HI		0.5	V
Logic 0	Voltage at PROG representing LO	2.2		V

9.2.2. Redundancy Decoding

If a bit is not fused properly (analogue readout levels violated), the redundancy bits can be used according the following table. Only one single bit can be overwritten with a logic HI. An improper fusing can not be made undone.

<15:12>	replaced bit		<15:12>	replaced bit
0000	none		1000	7
0001	0		1001	8
0010	1		1010	9
0011	2		1011	10
0100	3		1100	11
0101	4		1101	none
0110	5		1110	none
0111	6		1111	none

10 Polling Mode

Target of this mode is a reduction of the average power consumption. In this mode the IC supply is pulsed, thereby reducing the average power consumption to a fraction. The actual angle information and multi turn count value is not lost; polling mode is especially suited for battery powered applications. The IC is furthermore capable of generating a WAKE signal as soon as the magnet's position has changed. By means of the WAKE signal the system's power consumption can further be decreased if certain modules can be activated on demand.

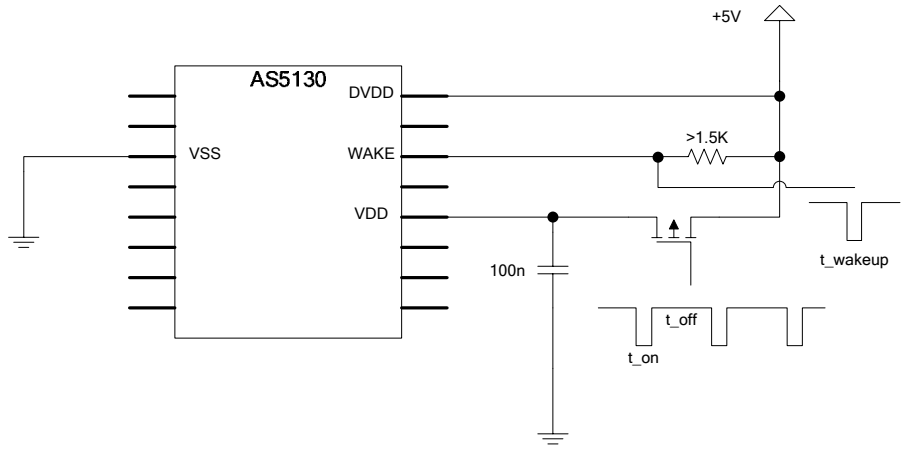


Figure 11: External circuitry for polling mode

The voltage at pin 16 (DVDD) determines whether polling mode is activated or not. Any voltage above 3.6V activates the polling functionality. This voltage must always be present at DVDD in order to hold the information in the registers.

The procedure is as follows:

- initial startup: the circuit starts up with invalid trim values, which are read back from the storage registers; the command rst_otp (command 19 – 10011) must be sent to read out valid trim values from the OTP
- these values are copied to the storage registers if OTP<8> (Wake enable) is set (must be set for polling mode)
- the values of AGC counter, actual angle, multi turn counter, hysteresis setting, wake threshold and gain setting are continuously updated in the storage registers
- the actual angle is stored as a reference by sending command STORE REF (command 3 – 00011). without this reference angle, a WAKE is generated at every startup
- the update of the storage registers is stopped if VDD drops below 4.45V and then the information is stored (DVDD) at the next startup (VDD on), the values are read back from the storage registers and the measured angle is compared with the stored reference angle; if the difference between both exceeds the threshold, a WAKE pulse is generated

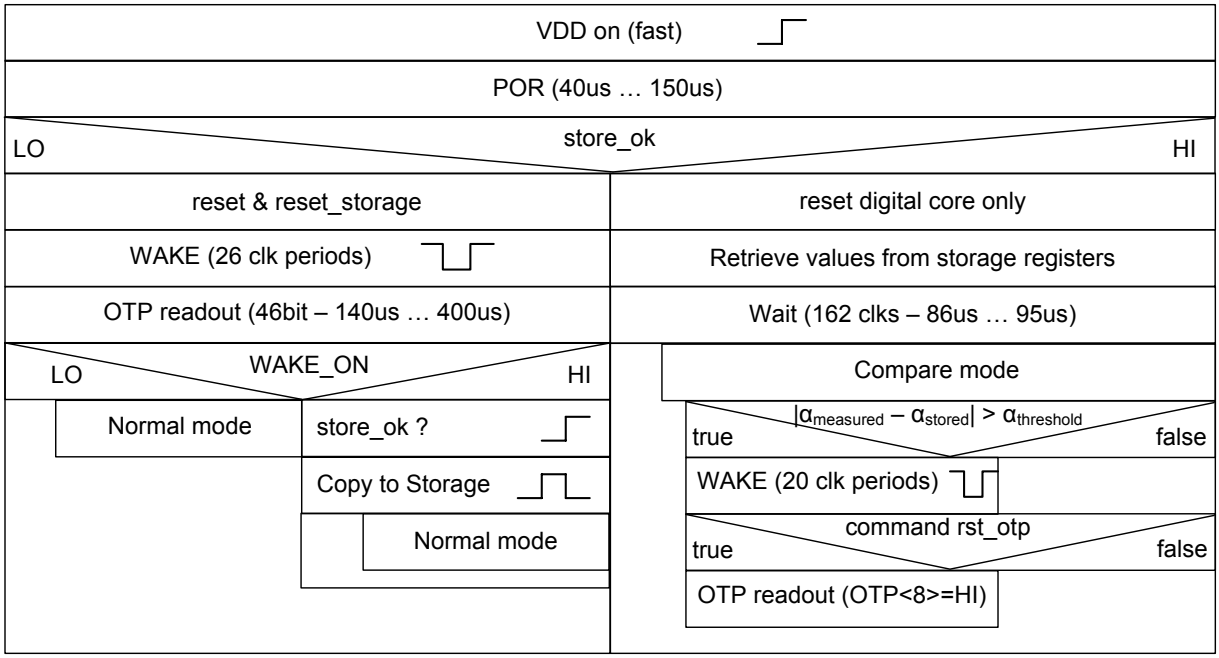


Figure 13 shows the behavior of the wake up signal. The wake up signal will be low for t_{wakeup} = 10us. After that, the wake up signal will go to tri-state condition. In case of an angle comparison with a result below the threshold, the signal will remain in tri-state condition.

(1) After switching on AVDD, the system needs max. 250us to generate an angle with maximum accuracy. A WAKE signal can not be expected until the end of this period.

10.1. WAKE Interface

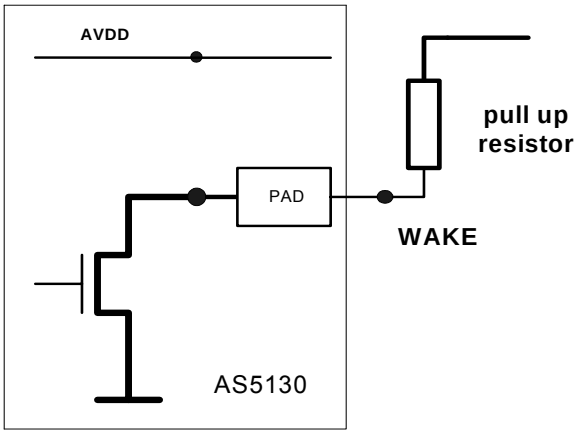


Fig. 12: WAKE output pin

An open drain NMOS structure is used in the WAKE pad. In order to generate a clear output signal level, a pull up resistor is required. The pad can drive 4mA.

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Pull up resistor	R_{pull_up}	1.5	100	kΩ	The used pad can drive 4mA.
Wake up pulse	$t_{wake\ up}$	10	17	µs	Interrupt signal to external devices, tri-state output, low active.
On-time	t_{on}	250	-	µs	Time for power up in polling mode. (1)
Off-time	t_{off}	-	-	ms	No limit unless DVDD is always supplied.

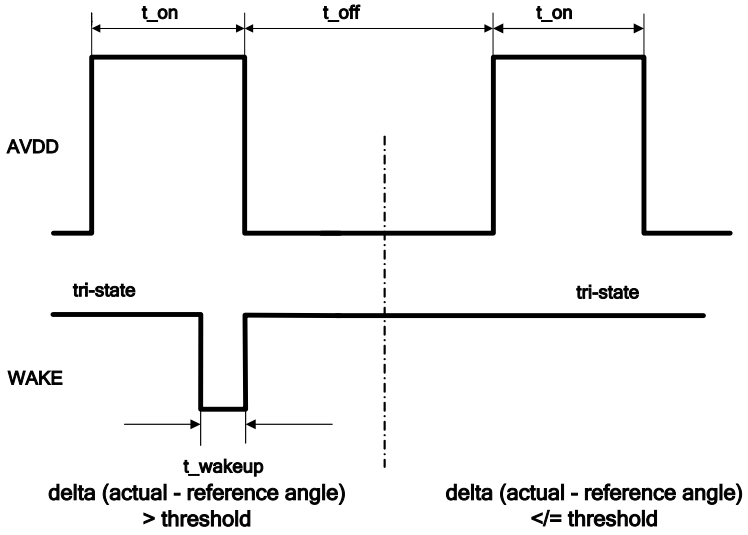


Fig. 13: wake up signal during polling mode of AVDD

11 Pulse Width Modulation Output (PWM)

The zero-corrected angle is linked also to another absolute interface. The pulse width modulated output provides a single wire interface which can be extended to an analogue output using an external RC filter (Target: Replacement of Potentiometer). The 8bit angle is decoded into the duty cycle of the pulsing output signal (see figure).

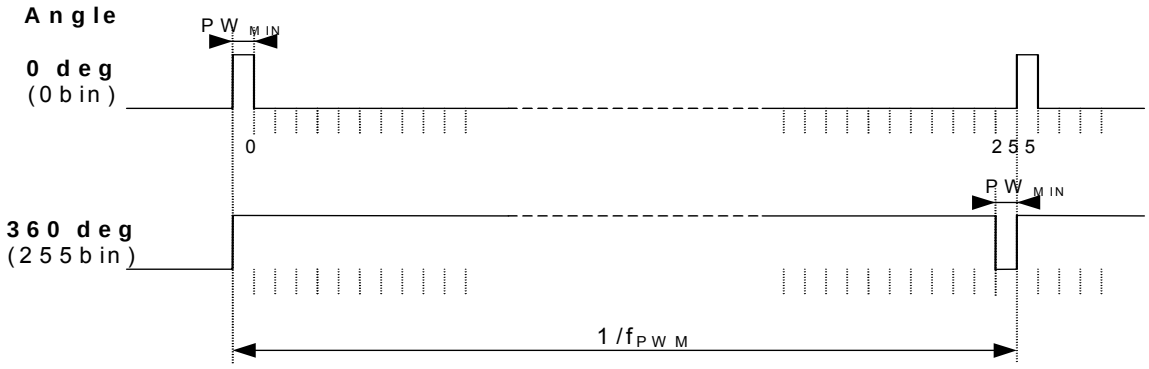


Fig. 14: PWM output parameter

The PWM output is generated by a 255 step periodic counter that runs at 1.8 MHz. The PWM signal will be generated from the currently stored angle information, Therefore this information is buffered and fixed until the next PWM-sequence is started. The PWM signal will only be generated if the stored angle information is valid (ADC locked, AGC not clamping).

As one high pulse before and one low pulse after the PWM data are needed as indicating signals, the pulse width is 257 / f_{ACLK}.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Analogue CLK (trimmed)	ACLK	1.7	1.8	1.9	MHz	Internal clock signal
PWM Frequency	f_{PWM}	6.6	7	7.4	kHz	
MIN Pulse Width	PW_{MIN}	0.52	0.56	0.59	µs	
MAX Pulse Width	PW_{MAX}	135	143	152	µs	

12 Multi Turn Counter

An 8 bit register is used for counting the magnet's revolutions. With each zero transition in any direction, the output of a special counter is incremented or decremented. The initial value after reset is 0 LSB.

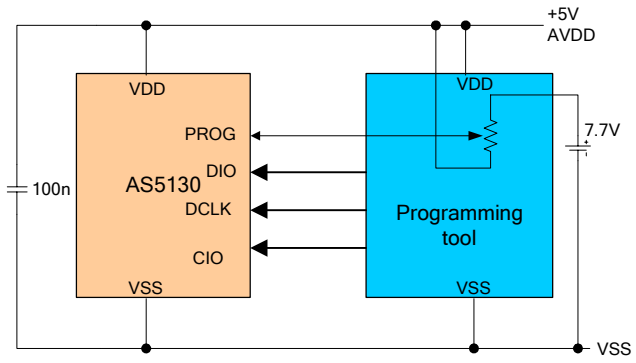
The multi turn value is encoded as complement on two. Clockwise rotation gives increasing angle values and positive turn count. Counter clockwise rotation exhibits decreasing angle values and a negative turn count respectively.

Bit Code	Decimal Value
01111111	127
…	…
00000011	+3
00000010	+2
00000001	+1
00000000	0
11111111	-1
11111110	-2
11111101	-3
…	…
10000000	-128

The counter output can be reset by using command 19 – HYST_RST. It is immediately reset by the rising clock edge of this bit. Any zero crossing between the clock edge and the next counter readout changes the counter value.

13 AS5130 Application Examples

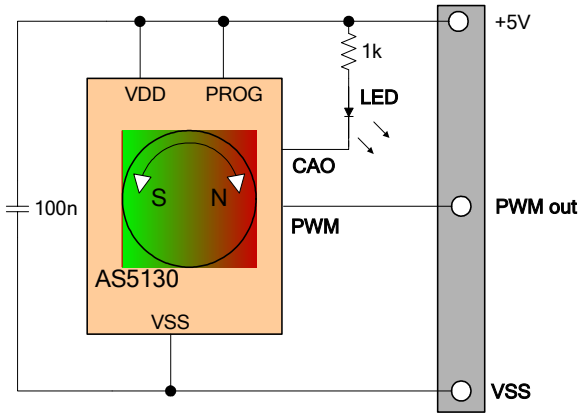
13.1 Application Example I



The AS5130 requires the serial interface via SSI for the programming of the OTP register. This configuration is recommended for applications, where the supply voltage for the AS5130 is shared among other parallel IC's during programming, such as a microcontroller.

Fig. 15: Programming via SSI serial interface

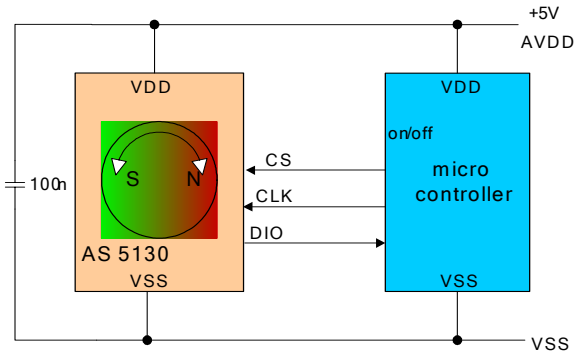
13.2. Application Example II 3-wire sensor with magnetic field strength indication



In Figure 12, a simple 360° sensor with PWM output is shown. The complete application requires only three wires, VDD, VSS and the PWM output. The circle over the center of the chip represents the diametrically polarized magnet. Additionally, the CAO pin will deliver an analog voltage indicating a missing magnetic field. This signal could be used to drive an external LED or to detect an alert signal.

Fig. 16: 3-wire angle sensor

13.3. Application Example III: Low-power encoder



Via SSI, the AS5130 will be able to toggle between active mode and low power mode. In active mode, the current consumption is ~15mA, in sleep mode 2mA. The fastest possible startup time from low power mode is 150µs. The AS5130 can be periodically switched between active and low power mode, the average power consumption depends on the duty cycle. In order to read out the correct data, the active mode time must be larger than 150µs.

Fig. 17: Low power encoder

Example: low power mode

$$I_{avg} = \frac{I_{active} * t_{on} + I_{power\_down} * t_{off}}{t_{on} + t_{off}}$$

Example: sampling period = one measurement every 10ms.
System constants = I_{active} = 15mA, I_{power_down} = 2 mA, t_{off} = 9,85ms, t_{on}(min) = 150µs (start-up from low power mode):

$$I_{avg} = \frac{15mA * 150\mu s + 2mA * 9{,}85ms}{150\mu s + 9{,}85ms} = 2.195mA$$

13.4. Application Example IV: Ultra-low-power encoder (polling mode)

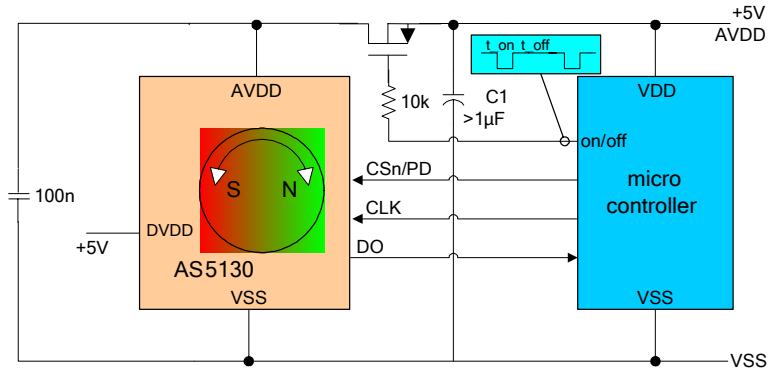


Fig. 18: Ultra low power encoder

Figure 18 shows a method to reduce the average power consumption even further.

Once powered up for at least 2.5ms, the AS5130 can be operated in a pulsed mode, where it is periodically turned on/off by a high side FET (PMOS) switching transistor with a low R_{on} (<10 Ohm). The on-time is at least 250µs in order to perform one measurement. A valid measurement result can be verified by checking the lock bit (ADC is locked) in the serial data stream.
After startup an OTP reset has to be performed in order to read out valid trimming information. Then a special SSI command (STORE REF) copies the actual angle into a buffered reference angle register. Now the AS5130 can be turned

off. Special registers will be buffered by the low power supply and will keep the actual settings. After a t_{on} of min. 250 us the actual angle is compared with the stored reference angle. If the angle difference is larger than a threshold value (wlsb, SSI command WRITE CUST), the AS5130 will send an interrupt request to an external device via the WAKE pin.
Due to the internal POR level of the IC, t_{on} starts after VDD has reached 4.3V (worst case POR level).

The average power consumption in this pulsed mode depends on the supply current in active mode and the duty cycle of the on/off pulse:

$$I_{avg} = \frac{I_{active} * t_{on}}{t_{on} + t_{off}}$$

Example: sampling period = one measurement every 100ms. System constants = I_{active} = 19mA, t_{on}(min) = 250µs:

$$I_{avg} = \frac{19mA * 250\mu s}{250\mu s + 99.75ms} = 47.5\mu A$$

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Contact Information

Headquarters
austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria
Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

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