

EL320.240-FA3

Operation Manual

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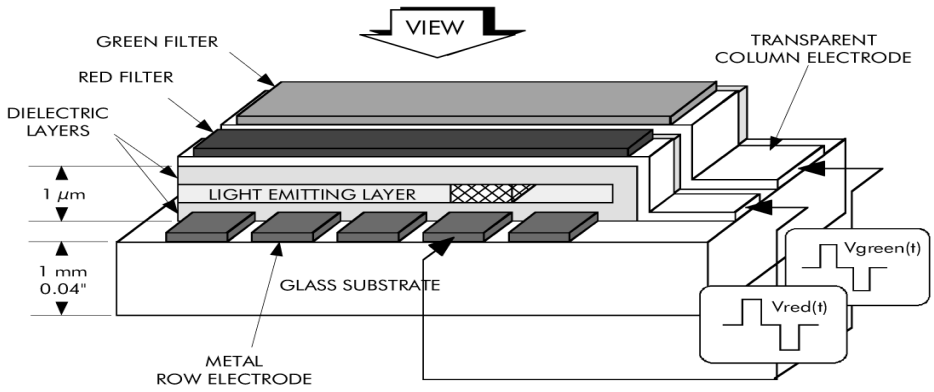
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1 EL320.240-FA3 multi-color QVGA display

The EL320.240-FA3 thin film electroluminescent (TFEL) multi-color display is a high-performance alternative to QVGA (320 x 240) LCDs and the ideal solution in demanding applications where superior visual performance, extreme temperature range, and environmental ruggedness are critical.

The EL320.240-FA3 utilizes Lumineq® Displays' proprietary Integral Contrast Enhancement (ICEBrite™) technology combined with red and green filters patterned over Lumineq Displays' industry-leading yellow phosphor to achieve unparalleled image quality in hues of red, green and yellow. Three intensity levels in each of the red and green sub-pixels generate 16 distinct colors (9 chromatically different colors, black, and 2 mid-levels of red, green, and yellow.)

The display consists of a solid state TFEL glass panel, depicted below, with a 124 mm diagonal active area, and control electronics assembled into a space-saving, rugged package for easy mounting.



1.1 Features and benefits

- Excellent visual performance:
  - Unparalleled crisp, clear image
  - Excellent contrast
  - Unbeatable viewing angle of > 179° for all colors in all directions
  - No off-axis color or contrast shift
- Extremely wide operation temperature range: -50°C to 85 °C
- Instant turn on at -50 °C: no heaters needed, no warm up time
- Long life phosphor: allows >11 years of continuous operation
- Wide dimming range via digital control and analog voltage input
- Rugged solid state construction
- Great reliability: MTBF > 50,000 hours demonstrated
- Low cost of ownership: no maintenance, no lamps to replace
- AMLCD-type panel interface, 3 V and 5 V logic compatible
- RoHS compliance

2 Installation and set-up

Do not drop, bend, or flex the display. Do not allow objects to strike the surface of the display.

CAUTION: The display uses CMOS and devices. These components are electrostatic-sensitive. Unpack, assemble, and examine this assembly in a static-controlled area only. When shipping, use packing materials designed for protection of electrostatic-sensitive components.

2.1 Mounting TFEL displays

Properly mounted, TFEL displays can withstand high shock loads as well as severe vibration found in demanding applications. However, the glass panel used in a TFEL display will break if subjected to bending stresses, high impact, or excessive loads.

Avoid bending the display. Stresses are often introduced when a display is mounted into a product. Ideally, the mounting tabs of the display should be the only point of contact with the system. Use a spacer or boss for support; failure to do so will bend the display and cause the glass to break. The instrument enclosure or frame should not flex or distort in such a way that the bending loads might be transferred to the display during use. The EL320.240-FA3 mounting tabs are designed for 3 mm screws. Mounting surfaces should be flat to within ±0.6 mm (±0.025"). Use all the mounting holes provided. Failure to do so will impair the shock and vibration resistance of the final installation.

WARNING: These products generate voltages capable of causing personal injury (high voltage up to 235 V_{AC}). Do not touch the display electronics during operation.

2.2 Cable length

A cable length of 0.5 m (20 inches) or less is recommended. Longer cables may cause visual artifacts, such as pixel “jitter”, due to data transfer problems between the host and the display.

2.3 Cleaning

As with any glass surface, care should be taken to minimize scratching. Clean the display glass with mild, water-based detergents only. Apply the cleaner sparingly to a soft cloth, then wipe the display. Disposable cleaning cloths are recommended to minimize the risk of inadvertently scratching the display with particles embedded in a re-used cloth.

2.4 Avoiding burn-in

As with other light-emitting displays, displaying fixed patterns on the screen may cause burn-in where luminance variations can be noticed after many hours of operation. To avoid image burn-in, use a screensaver or use periodic image inversion, if possible. Note that the rate of image burn-in will slow over time so that most of the burned-in image effect occurs in the first few hundred hours of operation.

2.5 Power supply and video sequencing and overcurrent protection

Any combination or sequencing in the application or removal of V_H (12 V_{DC} input power) and/or video signals will not result in abnormal display operation or display failure.

There is no overcurrent protection on V_H, the 12 V power input. To protect against catastrophic faults, Beneq recommends the use of a fuse or similar protection on the V_H input to the display.

2.6 Internal frame buffer

This display includes an internal frame buffer, which is required to transform the incoming video data into the desired displayed data. The display frame rate (the rate at which the phosphor is scanned) and thus the display brightness are independent of the frame rate of the user-supplied input data. Video data need not be continuously sent to the display since previously sent data is stored indefinitely until new data is received.

CAUTION: Some third-party video controllers use frame dithering algorithms to produce gray scale images. If such algorithms are used, the internal frame buffer may cause objectionable visual artifacts.

2.7 Color bit-mapping and color considerations

The EL320.240-FA3 utilizes standard AMLCD-type video interface timing. Thus, it is possible that a video source will be chosen. This provides 18 bits of data per pixel (6 bits each for red, green, and blue) as is common for AMLCD displays. Because the EL320.240-FA3 requires just 4 bits (two each for red and green) of data per pixel, the 18 bits would need to be mapped into 4 bits.

One option is to use just the two most significant bits of red and green and leave the rest open or terminated. This is the easiest approach and will work well if the user is developing their own content and can refrain from using patterns containing dim colors since these would be displayed as black. Another option is to electrically "OR" the 3 red MSBs together and route the result to R1, OR the 3 red LSBs together and route to R0, and do the same for G1 and G0. Additionally, the bits of blue could be ORd together with either the red or green bits depending on the characteristics of the images that need to be displayed.

If upgrading from a monochrome EL320.240 display model and using the SGD timing mode, some engineering effort will be required to map the monochrome SGD data into the color data required by the EL320.240-FA3. SGD data is one bit per pixel, and 4 pixels of data are latched per video clock edge. The EL320.240-FA3 is 4 bits per pixel with one pixel of data latched per clock edge.

Note that care must be taken when selecting colors for a given application to ensure that the selected colors are differentiated as desired. Although all fifteen colors and black are unique, some color levels are similar in chromaticity and/or luminance and typically should not be used together.

The colors in the following "color sets" are distinct but visually similar to each other: 1 & 2, 3 & 7, 4 & 8, 7 & 11, 5 & 6 & 9 & 10, and 13 & 14. For details, see the "Displayed colors" section of this manual.

In applications where the display is subject to physical motion or vibration, visual artifacts due to the gray scale frame dithering algorithm become more visible, especially in large blocks of color. For best results, use colors with no gray scale or 2/3 gray scale and the highest frame rate setting.

The following table lists the color levels which are dramatically distinct and most suitable for general use:

Color level	Color description	Similar color levels
3	Green	7
2	Medium Green	1
12	Red	None
8	Medium Red	4
15	Yellow	None
13	Orange	14
9	Brown Mustard	5, 6, and 10
11	Bright Neon Green	7
0	Black	None

2.8 Display overlay considerations

Though not a requirement, often the end system will employ some type of transparent cover over the front the display. The purpose and construction of the cover varies depending on the application and economical constraints. The cover may be used to improve contrast under certain lighting conditions by reducing reflections, to provide additional impact protection, to provide a more seamless enclosure appearance, or to protect against fluids. Some leading suppliers of display overlays are: EyeSaver International, Cyro Industries, and Dontech Incorporated.

3 Specifications and operation

3.1 Environmental

Environmental characteristics	
Temperature	
Operating	-50 °C to +85 °C
Storage	-50 °C to +105 °C
Humidity	
Non-condensing, operating	93 % RH max at +40 °C, per IEC 68-2-3
Condensing, non-operating	95 % RH max at +55 °C, per IEC 68-2-30
Altitude	
Operating/non-operating	0 to 18 km (58k ft) per IEC 68-2-13
Vibration	
Random	0.05 g^2/Hz, ASD level, 5-500 Hz per IEC 68-2-64,
Operating/non-operating	Test Fh.
Shock	
Operating/non-operating	100 g, 6 ms, half sine wave on each of six surfaces per IEC 68-2-27, test Ea.

3.2 Over-temp condition

The display contains a temperature sensor which measures the temperature of the circuit board at the lower left corner as viewed from the component side of the board.

If the board temperature exceeds approximately 100 °C, the display will automatically operate at its lowest luminance setting (as if LUM0 was low and LUM1 was high) to reduce the board temperature. At no point will the display be shut down. The content of the pattern will be unaffected.

After surpassing 100 °C, once the board temperature drops below approximately 92 °C (or the power is cycled), the display will resume normal operation as defined by the LUM0 and LUM1 settings. Typically, the 100 °C limit may be reached if the 12 V input power exceeds 6 W with the ambient temperature for the display electronics above 80 °C.

3.3 Optical

Optical characteristics		
Luminance		
Guaranteed	> 75 cd/m²	max frame rate (LUM0=LUM1=0), yellow, center
Typical	95 cd/m²	max frame rate (LUM0=LUM1=0), yellow, center
Guaranteed	> 41 cd/m²	min frame rate (LUM0=0, LUM1=1), yellow, center
Typical	53 cd/m²	min frame rate (LUM0=0, LUM1=1), yellow, center
Black luminance	< 0.2 cd/m²	max frame rate, 5 points: center plus four corners
Luminance non-uniformity		
Typical	5%	Max difference of two of five points (center plus four corners)
Luminance variation across temperature		
Maximum	±15%	Variation from 25 °C to the operating extremes
Luminance decrease over time		
Typical	6%	After 10,000 hours
Typical	15%	After 100,000 hours (> 11 years)
Viewing angle		
Minimum	>160° in all directions; no change to contrast, color, or luminance	
Contrast ratio		
Typical	1000:1	@ 0 lux ambient (dark room), maximum frame rate
	2.5:1	@ 20k lux ambient (daylight), maximum frame rate
	1.5:1	@ 75k lux ambient (direct sun), maximum frame rate

3.3.1 Displayed colors

The display can generate 16 colors based on red and green sub-pixels and frame dithering (utilizing a three frame period with either a 33% or 66% duty cycle.) Note that the colors in the following "color sets" are distinct but similar to each other in appearance: 1 & 2, 3 & 7, 4 & 8, 7 & 11, 5 & 6 & 9 & 10, and 13 & 14.

Color level	R1	R0	G1	G0	Pixel color description	Typical chromaticity (x, y coordinates)	FA1 red intensity	FA1 green intensity
0	0	0	0	0	Black	n/a	Off	Off
1	0	0	0	1	Dim Green	.450,.546	Off	1/3
2	0	0	1	0	Medium Green	.450,.546	Off	2/3
3	0	0	1	1	Green	.450,.546	Off	On
4	0	1	0	0	Dim Red	.606,.393	1/3	Off
5	0	1	0	1	Dim Yellow Brown	.497,.498	1/3	1/3
6	0	1	1	0	Greenish Brown	.481,.514	1/3	2/3
7	0	1	1	1	Neon Green	.471,.524	1/3	On
8	1	0	0	0	Medium Red	.606,.393	2/3	Off
9	1	0	0	1	Brown Mustard	.524,.473	2/3	1/3
10	1	0	1	0	Yellow Brown	.497,.498	2/3	2/3
11	1	0	1	1	Bright Neon Green	.480,.521	2/3	On
12	1	1	0	0	Red	.606,.393	On	Off
13	1	1	0	1	Orange	.535,.462	On	1/3
14	1	1	1	0	Bright Orange	.511,.485	On	2/3
15	1	1	1	1	Yellow	.497,.498	On	On

3.4 Power

The supply voltage and power requirements are shown in the table below. The power will vary greatly depending on the number of pixels lit and the chosen luminance level (see graph below.) Power levels will vary up to +/-15% from display to display due to brightness variation.

Table 1. Supply voltage and power requirements

Parameter	Minimum	Typical	Maximum	Abs max
Display supply voltage, V_H	8 V	12 V	18 V	
Supply current, with V_H = 8 V		0.59 A	1.16 A	1.44 A
Supply current, with V_H = 12 V		0.39 A	0.78 A	0.96 A
Power consumption @ maximum luminance (LUM0=LUM1=0)		4.7 W	9.3 W	11.5 W
Power consumption @ minimum luminance (LUM0=0, LUM1 =1)		3.1W	6 W	
Quiescent power consumption (SHUTDOWN = 1)		0.5 W		

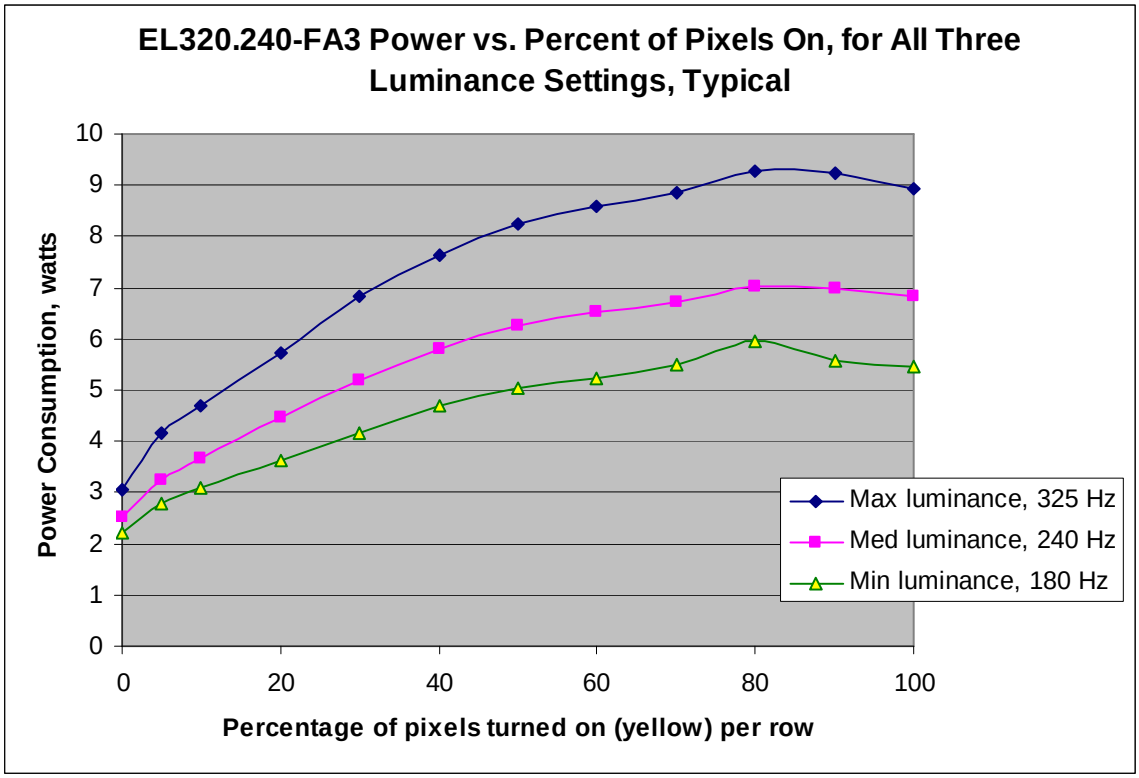
Note:

1) Maximum power condition: 80% of pixels lit (yellow) per row

2) Abs Max power: 80% of pixels lit (yellow) per row, worst case display sample

2) Typical power: pattern with 10% of pixels lit (yellow) per row, typical display

3) All power numbers are for LUMA open (no analog dimming)



3.5 Display interface

The display supports 5 video interface modes: SGD timing as used on the Beneq EL320.240.36-HB (though with video data differences to denote colors) and the 4 AMLCD timing modes used on Sharp and Kyocera QVGA color displays (though using only 2 bits of red and green data). 4 bits of data per pixel are provided. The data is clocked to the display with a video clock, VCLK. Frame and line synchronization is provided by the VS, HS, and (if needed) DE signals.

Video mode detection is performed automatically. The display evaluates the timing of the incoming video approximately every 25 ms and will shift "on the fly" between video modes as required.

The internal display controller utilizes a frame buffer to provide the display with the appropriate modulation on a line-by-line and frame-by-frame basis to implement the color generation, including frame dithering algorithms. Thus, the input frame rate and the display scan rate, in general, will not be the same and will not be synchronous.

3.5.1 Video mode selection

Inputs LUM0 and LUM1 must be set to attain the desired video mode as shown in the following table.

LUM0 and LUM1 = 1?	V/Q input	DE input	Mode name	Mode description (refer to video mode timing for details)
No	0	Active	AMLCD, QVGA	AMLCD timing. DE determines the horizontal location of data.
No	0	0	AMLCD, QVGA, Fixed	AMLCD timing. Horizontal start of valid data is a predetermined number of VCLKs from HS.
No	1	Active	AMLCD, VGA	AMLCD timing. Displays the upper left quadrant of a VGA (640x480) input signal with DE determining the horizontal location of data.
No	1	0	AMLCD, VGA, Fixed	AMLCD timing. Displays the upper left quadrant of a VGA (640x480) input signal with the horizontal start of valid data predetermined.
No	X	1	SGD	SGD timing. Horizontal start of valid data is the first VCLK after HS.
Yes	X	X	Self test	Displays various patterns at the maximum refresh rate regardless of video input data. Useful for verifying display functionality.

Note:

1) DE is considered active if more than 8 logic transitions are detected.

2) SGD mode is similar to that of the Lumineq EL320.240.36 and EL320.240-HB displays, but with required changes to the video data content to represent color.

3) The AMLCD modes are compatible with those found on the following QVGA displays though the video data content of 4 bits/pixel is a subset of the typical 18 bits/pixel: Sharp LQ057Q3DC12, Sharp LQ057Q3DC02, Kyocera TCG057QV1AC.

3.5.2 Connector

The display uses the Samtec EHT-110-01-S-D or equivalent 2 mm locking connector. The mating connector is in the Samtec TCSD family of cable strips. The proper connector, user-specified cable length and connector configuration is supplied as a single unit. Consult your Samtec representative for the cable/connector options. Compatibility with non-Samtec equivalents should be verified before use.

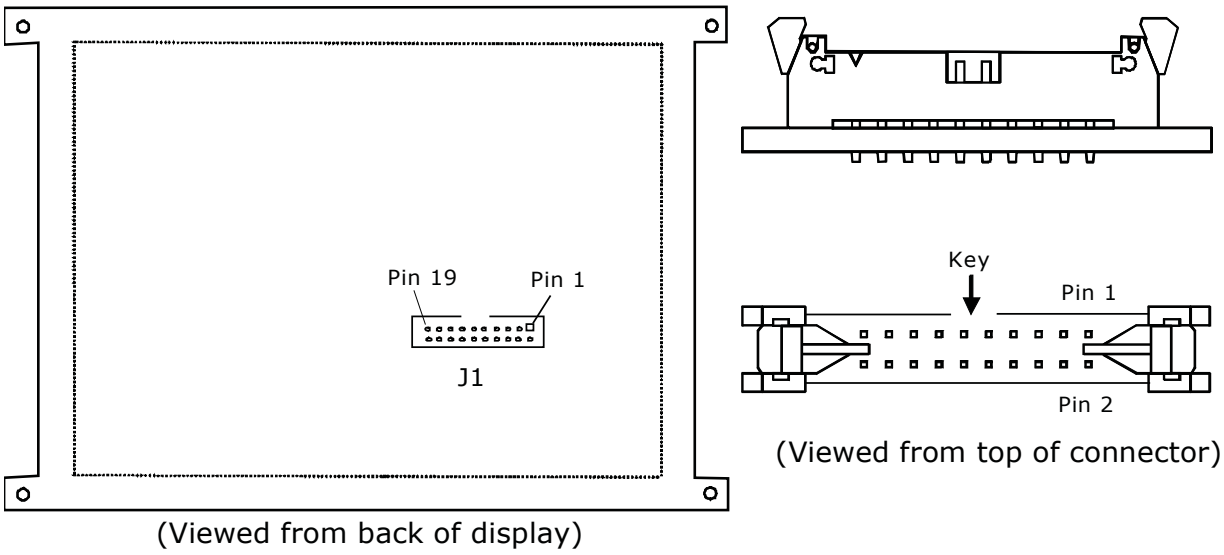


Figure 1. Data/power connector

Table 2. J1 Connector pin assignment

Signal	Pin	Pin	Signal
V_H	1	2	V_H
V/Q	3	4	DE
LUMA	5	6	LUM0
VS	7	8	LUM1
HS	9	10	GND
VCLK	11	12	GND
R0	13	14	GND
R1	15	16	GND
G0	17	18	GND
G1	19	20	SHUTDOWN

3.5.3 Display input descriptions

Signal	Description
V_H	Power supply voltage for display functions. 12 VDC nominal.
V/Q	Format selection: in AMLCD timing modes, selects between VGA mode (high) and QVGA mode. In VGA mode, the upper left quadrant of data will be displayed. Internally pulled low.
DE	Data Enable: in AMLCD non-fixed timing modes, the rising edge identifies the data for the first pixel of each row and must stay high until the data for the last pixel of each row is clocked. DE is also used to determine the video timing mode. Internally pulled high to 3.3 V.
LUMA	Analog Luminance Control: used to reduce the display luminance by reducing the voltage applied to the display phosphor. If left open, defaults to the luminance set by LUM0 and LUM1.
LUM0, LUM1	Digital Luminance Controls: used to reduce the luminance of the display by reducing the frequency at which the display is scanned.
VS	Vertical Sync: identifies the start of each frame (entire screen) of data. Internally pulled low.
HS	Horizontal Sync: identifies the start of each horizontal row of data.
VCLK	Video Clock: the falling edge latches the video data (R0, R1, G0, and G1).
R0	Video data: Least significant bit for red sub-pixel.
R1	Video data: Most significant bit for red sub-pixel.
G0	Video data: Least significant bit for green sub-pixel.
G1	Video data: Most significant bit for green sub-pixel.
SHUTDOWN	Display Shutdown: when high, will disable the display, thus rendering the display black and minimizing power. All display data will be stored but no new data accepted when SHUTDOWN is high. Internally pulled low.
GND	Signal return for power and logic.

Table 3. Logic signal requirements

Description	Min	Max	Units	Notes
Absolute input logic voltage range	-0.3	5.5	V	For all inputs except V_H, LUMA
Logic high voltage	2.0	5.5	V	All input thresholds are TTL
Logic low voltage	-0.3	0.8	V	All input thresholds are TTL
LUMA input voltage	0	5.5	V	Leave open if not used
LUMA input current	-250	0	µA	

Note:

1. All logic inputs (except LUMA input) are 5 V tolerant, with 270 Ω series resistors.
2. Input capacitance for all logic inputs except LUMA is 8 pF typical.
3. DE, LUM0, and LUM1 have > 20 kΩ pull-up resistors to 3.3 V.
4. VS, SHUTDOWN, and V/Q have > 20 kΩ pull-down resistors to ground

3.5.4 Video mode timing—SGD video mode

Item	Description	Min.	Max.	Units
1	HS high time	30		ns
2	Last VCLK fall to HS fall	20		ns
3	HS to VCLK rising edge	10		ns
4	R/G data setup to VCLK	10		ns
5	R/G data hold from VCLK	10		ns
6	VCLK period	100		ns
7	VCLK low width	30		ns
8	VCLK high width	30		ns
9	VS high setup to HS low	140		ns
10	VS hold after HS	140		ns
11	VS low setup to HS high	140		ns
12	HS period	34		µs
	VS period	240		HS periods
	VS frequency		120	Hz

Notes:

1) The first HS falling edge occurring when VS is high indicates the first row.

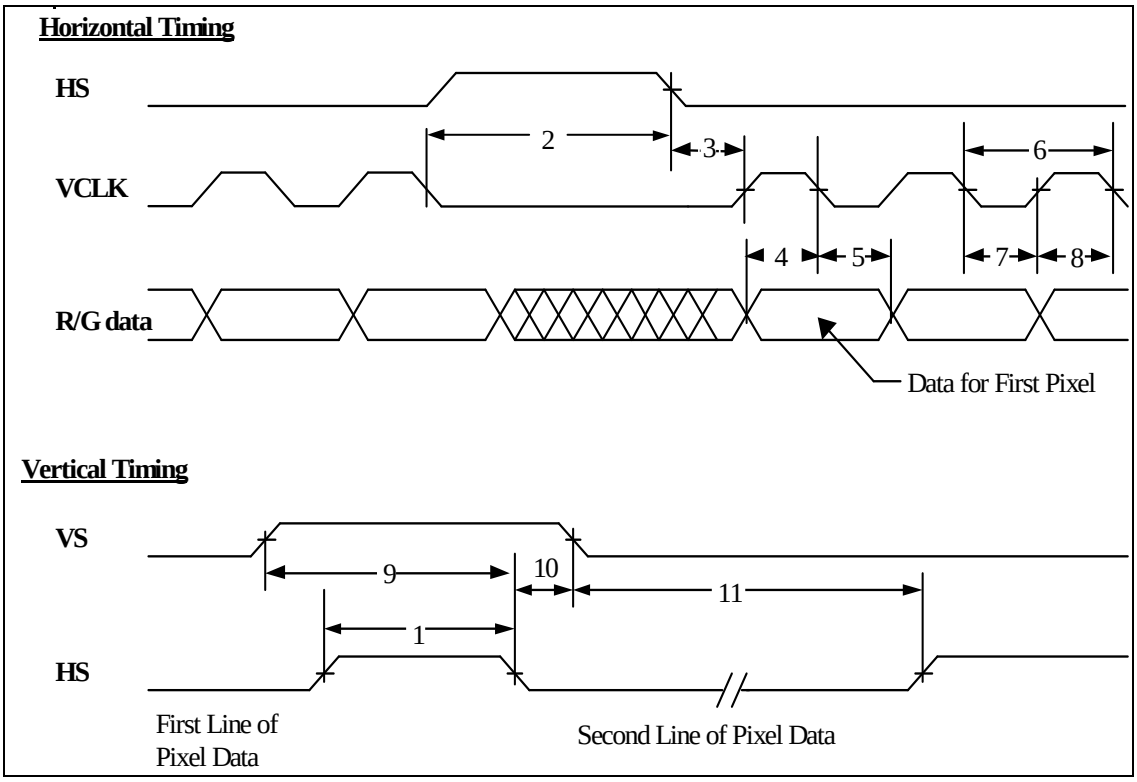
2) The video data for a given row is clocked in prior to the falling edge of HS.

3) The first 320 VCLK falling edges after the fall of HS clock in the valid data.

4) If video inputs are halted, the previously clocked in data will be displayed.

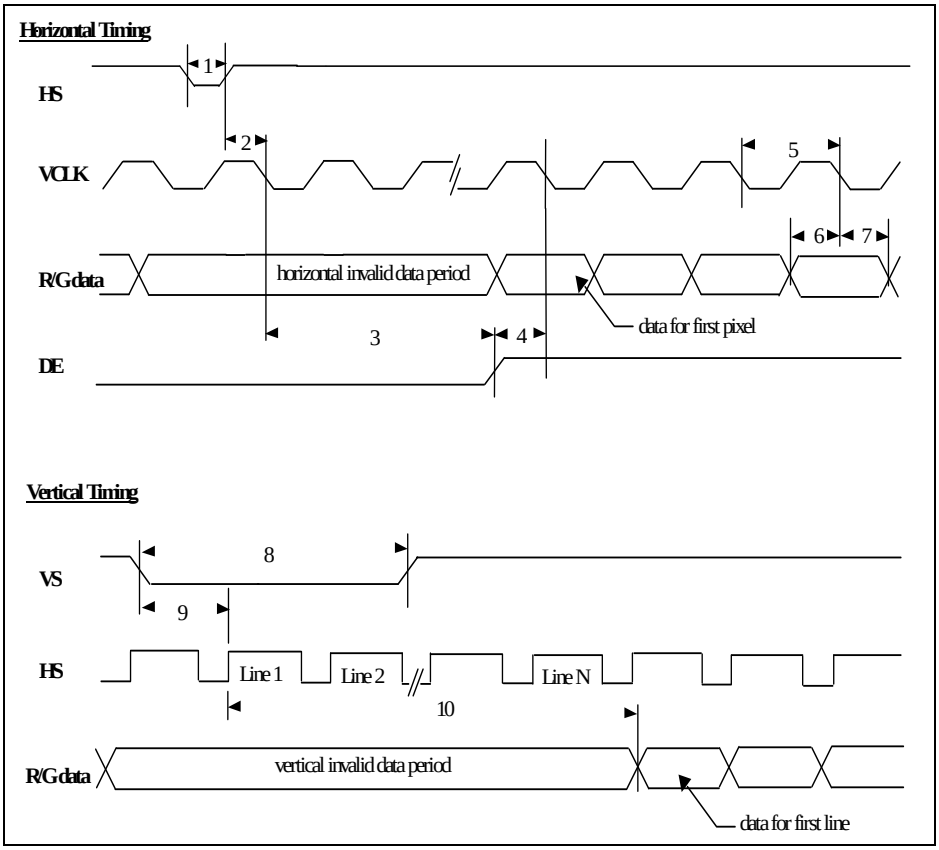
5) Video frame dithering/gray scale may cause artifacts due to the frame buffer.

6) All timing measurements are made at 1.6 V.



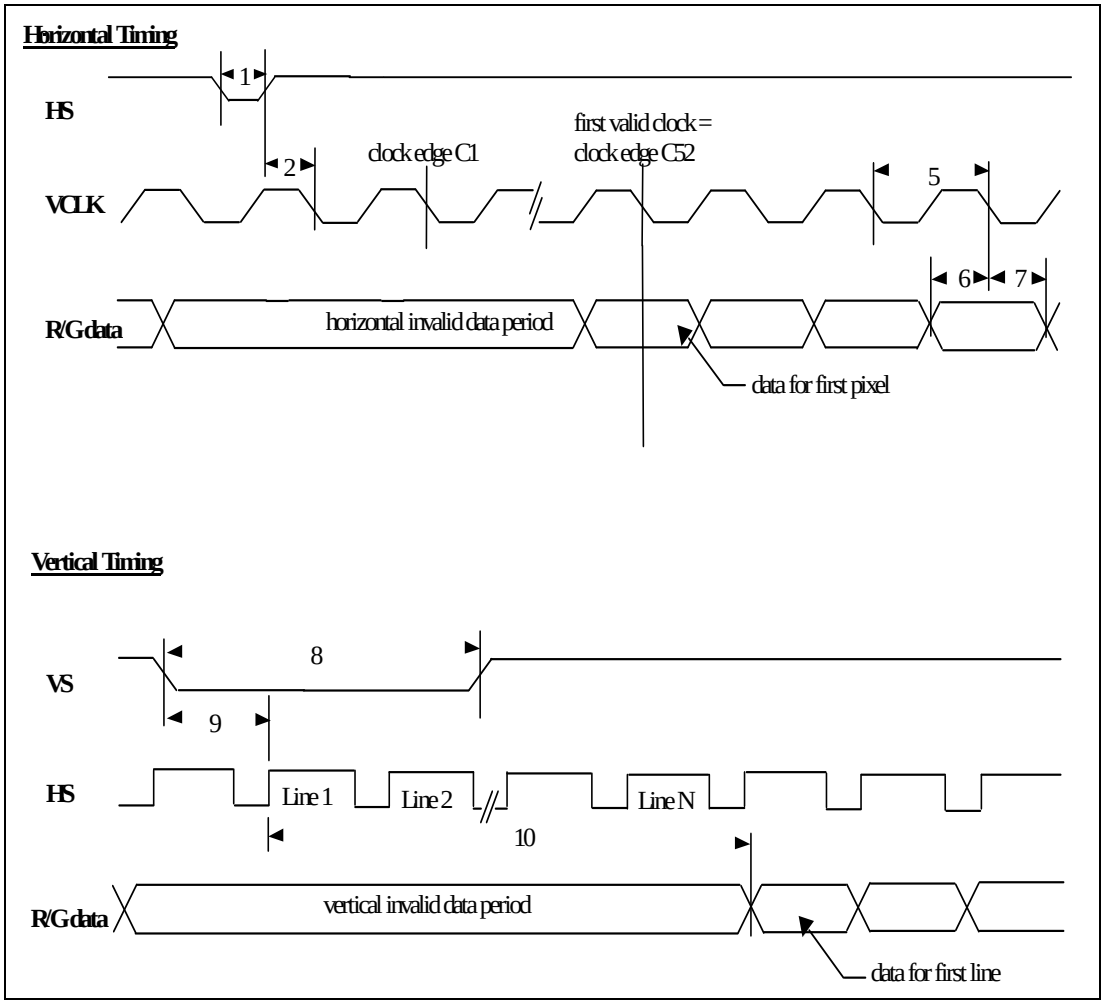
3.5.5 Video mode timing—AMLCD video mode, QVGA

Item	Description	Min.	Max.	Units
1	HS low time	2	200	VCLK periods
2	HS to VCLK phase difference	10	VCLK period - 10	ns
3	HS to DE phase difference	2	HS period - 340	VCLK periods
4	DE set up time	5	VCLK period - 10	ns
5	VCLK frequency		7	MHz
6	R/G data set up to VCLK	5		ns
7	R/G data hold from VCLK	10		ns
8	VS low width	2	34	HS periods
9	VS to HS phase difference	0	HS period – HS low time	ns
10	Vertical start position	After 7 HS rising edges		
	DE high time	2	HS period - 10	VCLK periods
	HS period	50		µs
	VS period	251	280	HS periods



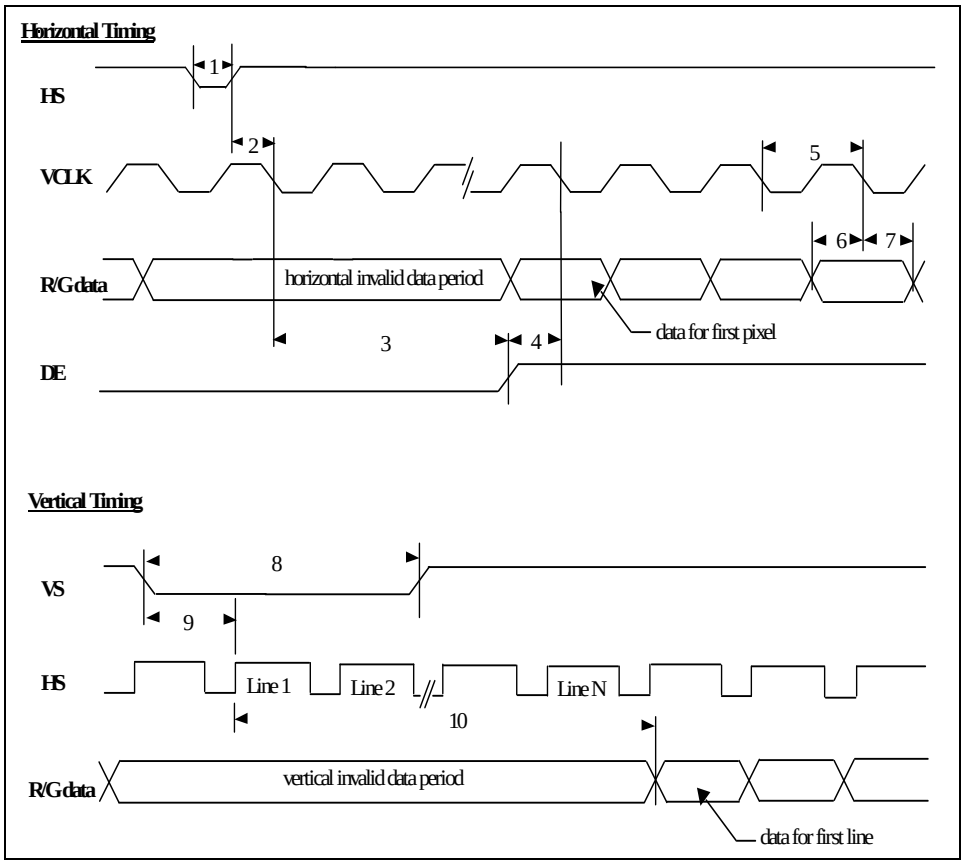
3.5.6 Video mode timing—AMLCD video mode, QVGA, fixed

Item	Description	Min.	Max.	Units
1	HS low time	2	200	VCLK periods
2	HS to VCLK phase difference	10	VCLK period - 10	ns
5	VCLK frequency		7	MHz
6	R/G data set up to VCLK	5		ns
7	R/G data hold from VCLK	10		ns
8	VS low width	2	34	HS periods
9	VS to HS phase difference	0	HS period – HS low time	ns
10	Vertical start position	After 7 HS rising edges		
	HS period	50		µs
	VS period	251	280	HS periods



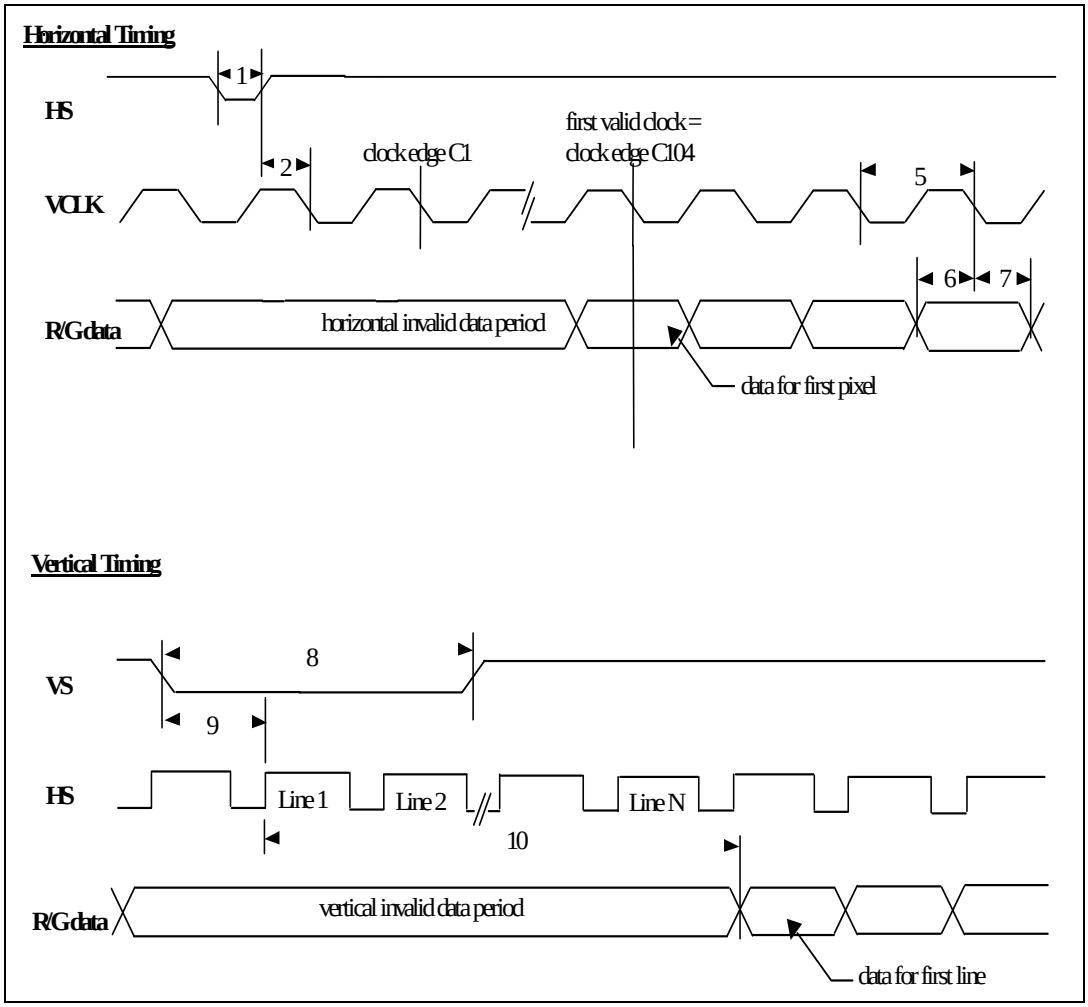
3.5.7 Video mode timing—AMLCD video mode, VGA

Item	Description	Min.	Max.	Units
1	HS low time	2	200	VCLK periods
2	HS to VCLK phase difference	10	VCLK period - 10	ns
3	HS to DE phase difference	44	HS period - 664	VCLK periods
4	DE set up time	5	VCLK period - 10	ns
5	VCLK frequency		28.33	MHz
6	R/G data set up to VCLK	5		ns
7	R/G data hold from VCLK	10		ns
8	VS low width	2	34	HS periods
9	VS to HS phase difference	0	HS period – HS low time	ns
10	Vertical start position	After 34 HS rising edges		
	DE high time	2	HS period - 10	VCLK periods
	HS period	30		µs
	VS period	515	560	HS periods



3.5.8 Video mode timing—AMLCD video mode, VGA, fixed

Item	Description	Min.	Max.	Units
1	HS low time	2	200	VCLK periods
2	HS to VCLK phase difference	10	VCLK period - 10	ns
5	VCLK frequency		28.33	MHz
6	R/G data set up to VCLK	5		ns
7	R/G data hold from VCLK	10		ns
8	VS low width	2	34	HS periods
9	VS to HS phase difference	0	HS period – HS low time	ns
10	Vertical start position	After 34 HS rising edges		
	HS period	30		µs
	VS period	515	560	HS periods



3.6 Dimming

Dimming is used to reduce the display luminance to better match ambient conditions or to reduce power consumption. There are two methods for dimming the EL320.240-FA3 display.

The preferred method is digital dimming, where the internal display frame rate is controlled using the LUM0 and LUM1 inputs. The internal frame rate is the frequency at which the drive voltage is applied to the display phosphor and thus impacts luminance and power consumption. Note that the internal display frame rate is unrelated to the frame rate defined by the VS input.

(For normal operation, LUM0 and LUM1 must not be open or both high. When LUM0 and LUM1 are high or open, the display enters the self-test mode where pre-determined patterns are displayed.)

Using the combination of the two inputs LUM0 and LUM1, the following display luminance settings are obtained:

Table 4. Digital luminance control characteristics

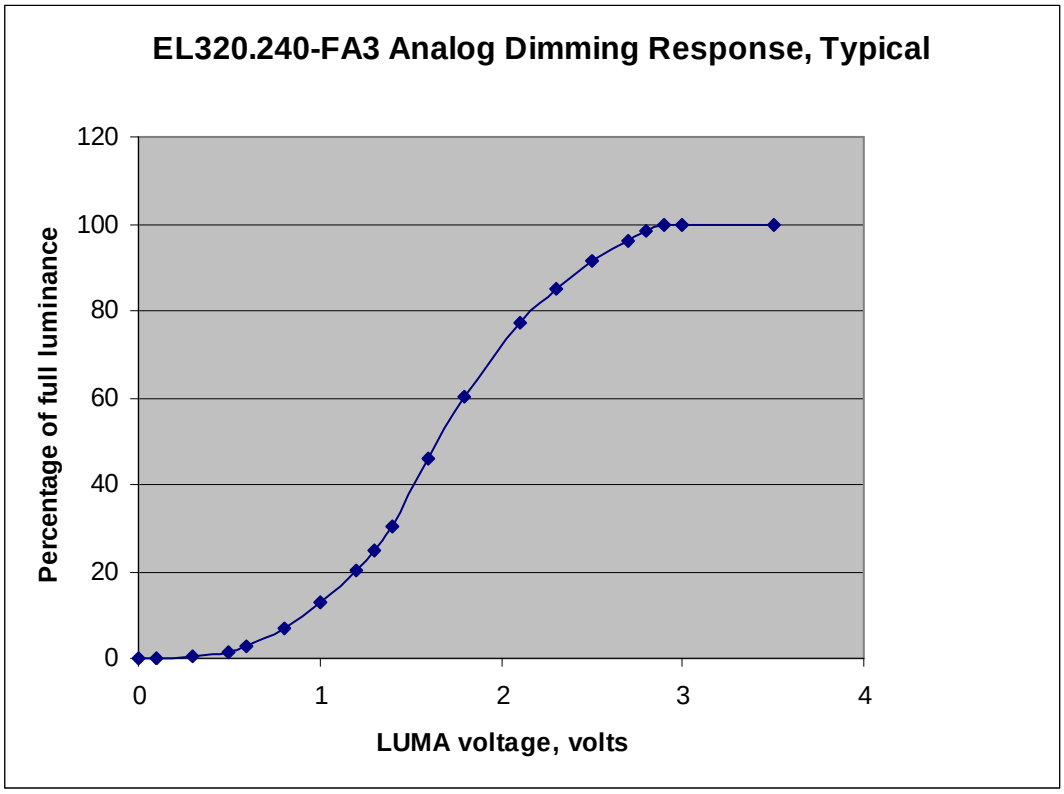
LUM0 logic level	0	1	0
LUM1 logic level	0	0	1
Approximate frame rate, Hz	325	240	180
Approximate relative luminance	100%	74%	55%

If the dimming obtained from digital dimming is insufficient, analog luminance control (the LUMA input) may be used to adjust the luminance further downward. Connection of a 50 kΩ variable resistor between LUMA and GND will give a brightness range of approximately < 5% to 100% of the full luminance value (see dimming curve below). Alternatively, an external voltage or D/A converter may be used to sink current from LUMA to GND.

Table 5. Analog luminance control characteristics

Max luminance, LUMA open	100% (no dimming)
Max luminance, 50 kΩ from LUMA to GND	100%
Min luminance, 0 Ω from LUMA to GND	0.2% typical, 5% maximum
LUMA open circuit voltage	4 V, nominal
LUMA maximum sink current	250 µA

When using LUMA for dimming, visual artifacts, such as brightness non-uniformity and image burn-in, may become more noticeable especially at low dimming levels. In addition, colors created by mixing red and green sub-pixels may chromatically shift. To minimize the visual artifacts, analog dimming should be employed with LUM0 and LUM1 set for the minimum frame rate. See the following graph for the typical analog dimming response. Note that the actual response may vary depending on the individual display.



3.7 Self-test mode

The display contains a self-test mode composed of patterns displayed at the maximum frame rate for approximately four seconds each. Self-test mode can be useful for verifying operation of the display.

The self-test patterns are as follows: yellow diagonal lines with a one sub-pixel wide perimeter box, all pixels red, all pixels green, and all pixels yellow. Upon power up when in the self-test mode, the pattern sequences are repeated three times and then the pattern remains in the all pixels yellow state. The self-test mode is entered by leaving LUM0 and LUM1 disconnected or logically high.

3.8 Reliability

The display MTBF is to be greater than 50,000 hours at maximum luminance and maximum input power with a 90% confidence level at 25 °C.

3.9 Safety and EMI performance

The display will not inhibit the end product from obtaining these certifications: IEC 60101-1; UL60950; CSA 22.2 IEC950; FCC Part 15, Subpart J, Class B; EN55022 Class B.

3.10 Mechanical characteristics

Mechanical characteristics		
Display external dimensions		
millimeters (inches)	width	150.3 (5.92)
	height	104.8 (4.13)
	depth	20.56 max (0.81)
Weight (typical)	198 g	
Display active area		
millimeters (inches)	width	99.15 (4.05)
	height	74.36 (2.93)
	diagonal	123.94 (4.88)
Pixel size		
millimeters (inches)	width	0.265 (0.010)
	height	0.265 (0.010)
Pixel pitch		
millimeters (inches)	width	0.31 (0.012)
	height	0.31 (0.012)

3.10.1 Display dimensions and component envelope

The figure below shows the display dimensions. For additional details, the Mechanical Outline drawing is available at www.beneq.com.

Note the 20.56 mm component envelope. This is the depth required by the display to ensure no interference with display board components, which are up to 12.19 mm in height (above the board surface.) While tall components are the minority, Beneq reserves the right to relocate components within the constraints of the component envelope without prior customer notification. For this reason, Beneq advises users to design enclosure components to be outside the component envelope.

Device designers will need to consider their specific system requirements to determine the spacing necessary to maintain the specified ambient temperature for the display electronics.

Air flow and the thermal properties of the surrounding components will impact the required depth of the air gap. In addition, electrical spacing must be considered to accommodate the high voltage (up to 235 V_{DC}) present on the display electronics.

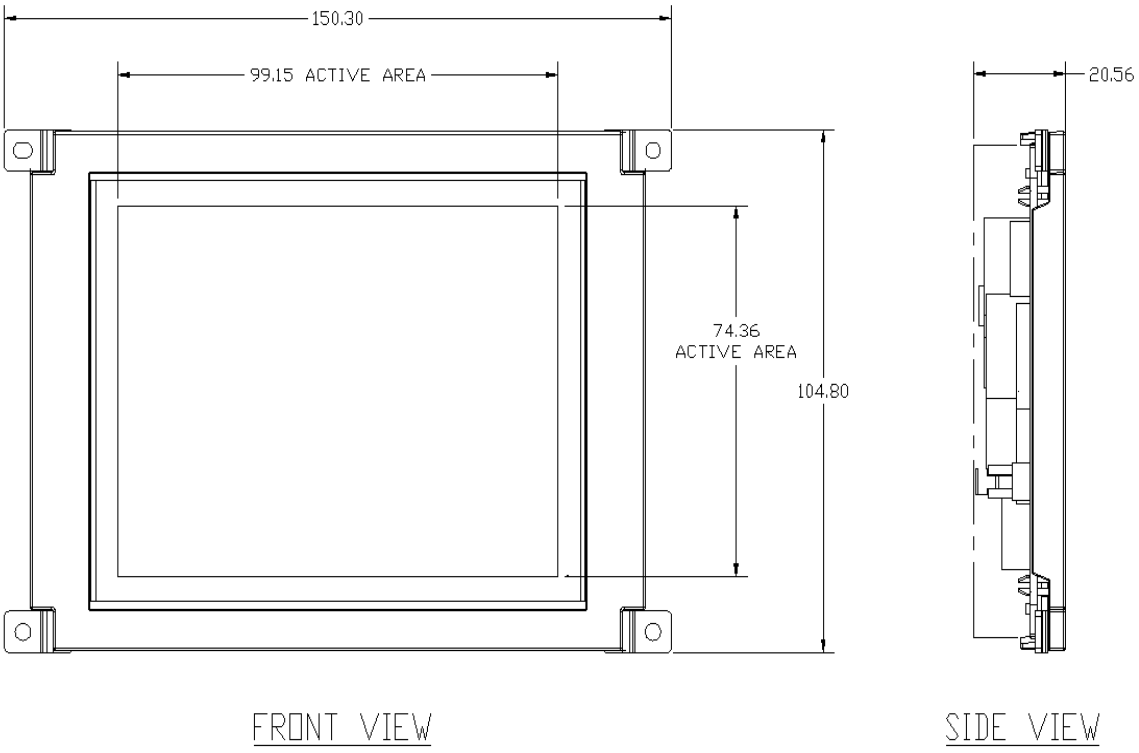


Figure 2. Display dimensions (millimeters, ±0.25 mm)

4 Description of warranty

Seller warrants that the Goods will conform to published specifications and be free from defects in material during warranty time from delivery. To the extent that goods incorporate third-party-owned software, seller shall pass on seller's licensor's warranty to buyer subject to the terms and conditions of seller's license.

Warranty repairs shall be warranted for the remainder of the original warranty period. Buyer shall report defect claims in writing to seller immediately upon discovery, and in any event, within the warranty period. Buyer must return goods to seller within 30 days of seller's receipt of a warranty claim notice and only after receiving seller's return goods authorization. Seller shall, at its sole option, repair or replace the goods.

If goods were repaired, altered or modified by persons other than seller, this warranty is void. Conditions resulting from normal wear and tear and buyer's failure to properly store, install, operate, handle or maintain the goods are not within this warranty. Repair or replacement of goods is seller's sole obligation and buyer's exclusive remedy for all claims of defects. If that remedy is adjudicated insufficient, Seller shall refund buyer's paid price for the goods and have no other liability to buyer.

All warranty repairs must be performed at seller's authorized service center using parts approved by seller. Buyer shall pay costs of sending goods to seller on a warranty claim and seller shall pay costs of returning goods to buyer. The turnaround time on repairs will usually be 30 working days or less. Seller accepts no added liability for additional days for repair or replacement.

If seller offers technical support relating to the goods, such support shall neither modify the warranty nor create an obligation of seller. Buyer is not relying on seller's skill or judgment to select goods for buyer's purposes. Seller's software, if included with goods, is sold as is, and this warranty is inapplicable to such software.

SELLER DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

5 Ordering information

Product	Part number	Description
EL320.240-FA3	997-3377-00LF	Standard FA3 display.
EL320.240-FA3 CC	997-3377-01LF	Same as standard FA3, but with the electronics conformal coated (acrylic material: HumiSeal p/n 1B73) to minimize the effects of moisture and conductive debris

Design and specifications are subject to change without notice.

Beneq Systems continues to provide optional, and in many cases custom, features to address the specific customer requirements. Consult Beneq Sales for pricing, lead time and minimum quantity requirements.

6 Support and service

Beneq Oy is a Finnish company based in Espoo, Finland, with a world-wide sales distribution network. Full application engineering support and service are available to make the integration of Lumineq displays as simple and quick as possible for our customers.

RMA Procedure: For a Returned Material Authorization number, please contact Beneq Oy by email (rma.lumineq@beneq.com) with the model number(s), serial number(s) and brief description of the problem. When returning goods for repair, please include a brief description of the problem, and mark the outside of the shipping container with the RMA number.

7 RoHS II

Beneq Oy is committed to continuous improvement. As part of this process we are fully in support of EU directive 2011/65/EU, the Restriction of Hazardous Substances, commonly known as RoHS II or RoHS Recast, which, compared to RoHS, keeps the restrictions on the original six hazardous substances, including lead (Pb) in electronic equipment. It also expands these restrictions to previously exempted categories including medical devices and monitoring and control instruments.

Beneq part number with an "LF" suffix designation indicates RoHS compliance, as shown on the part number label affixed to the display and on the box containing the display.

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